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The LTC1410 Converts Twelve Bits at 1.25MSPS

by Dave Thomas

Introduction

Until now, designers of high-speed data acquisition systems have had to make some tough compromises when picking 1MSPS 12-bit A/D converters. The parts with the best performance were hybrids in large packages, which consumed 1W or more and cost $100.00 or more. A few manufactures offered monolithic solutions, but they didn't perform as well as hybrids. Some of the monolithic parts had poor AC performance but good DC performance, whereas others had good AC and inferior DC performance. Now, LTC has a monolithic, 1.25MSPS 12-bit ADC with the performance of the best hybrids but with the power, size, and cost of a monolithic part. Some of the key features of this new device include:

- ❏ 1.25 MSPS throughput
- ❏ Low-power—150mW typical from 5V supplies
- ❏ NAP and SLEEP power-shutdown modes
- ❏ Small package—28-pin SSOP

Not only does this device match or beat the performance of expensive hybrids, it also offers some new features they never had, like true differential inputs and two power shutdown modes. These features can help improve the performance of current data-acquisition systems and open up new applications that were not previously possible because of high power consumption.

High-Accuracy Conversions: AC or DC

Figure 1 is a block diagram of the LTC1410. A high-performance differential sample-and-hold circuit combined with an extremely fast, successive-approximation ADC and an on-chip reference deliver a previously unattainable combination of AC and DC performance. A digital interface allows easy connection to microprocessors, FIFOs, or DSPs.

The DC specifications include a 0.8LSB maximum differential linearity error and 0.5LSB maximum integral linearity error guaranteed over temperature. The gain of the ADC is held nearly constant over temperature with an on-chip 10ppm/°C curvature-corrected bandgap reference.

The sample-and-hold circuit sets the dynamic performance of the ADC. The LTC1410 has a wide bandwidth and very low distortion differential sample-and-hold. Specifications include total harmonic distortion of –84dB for a 625kHz input and an input bandwidth of 30MHz for the sample-and-hold.

High-Impedance Inputs Speed Data Acquisition

High speed ADCs are often used to sample many different channels in multiplexed systems. The LTC1410 is well suited to these applications. The high-impedance inputs are easy to switch through a MUX without

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Remembering the Six-Transistor Radio

by Richard Markell

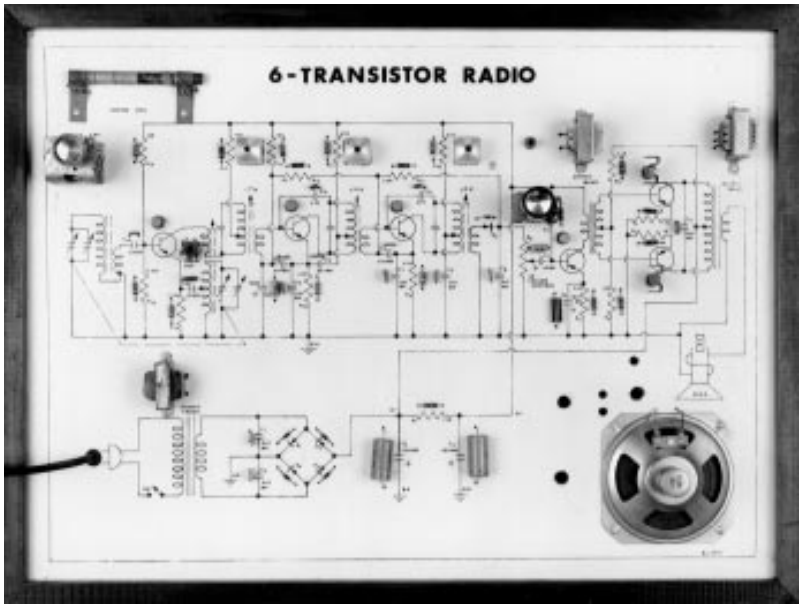

Figure 1. The classic six-transistor radio

How many years has it been since the demise of the six-transistor radio? How many of us at LTC remember our electronics class in junior high school or even high school? I have fond memories of walking around the neighborhood with my crystal radio, testing water pipes, fences, metal-framed buildings, and the tree next to my window, to see which would give the best reception.

Nerd visions of the past? Perhaps, but I think winding a tuning coil on a used toilet paper roll teaches one more than calling up the "coil" icon in Crystal RadioBuilder for Windows™. The six-transistor radio (Figure 1) was not only a great tool for learning electronics, but it taught many "teeners" how to troubleshoot and, perhaps, even how to think. I hope today's kids have their equivalent of the six-transistor radio.

★ ★ ★

Our lead article highlights the LTC1410, a new 12-bit, 1.25MSPS analog-to-digital converter specifically designed for both AC and DC accuracy. This part consumes only 150 milliwatts from a ±5 volt supply. We also introduce three new digital-to-analog converters, the LTC1451, LTC1452, and LTC1453. These parts bring 12-bit performance, single-supply operation, and rail-to-rail voltage output performance using a three-wire serial interface to the ever-growing LTC product line.

The LTC1472, a complete V_{CC} and VPP PCMCIA switch-matrix IC is the subjects of a feature article. This issue also introduces several new switching regulators. The LTC1266 is a synchronous, step-down switching regulator that can drive two external, N-channel MOSFETs. The LTC1266 can achieve high efficiency at loads to 10A or more. The LTC1265 is a step-down converter in a 14-pin SOIC package, capable of operating at frequencies to 700kHz, that can supply output currents up to 1.2 Amps. The LTC1265 requires only 160 microamps of quiescent current, which decreases to only 5 microamps in shutdown conditions.

The LTC1267 is a dual switching-regulator controller with extremely wide, 4V-to-40V input operating range and reduced supply currents. This dual controller provides efficiencies better than 90% in a space-saving 28-pin SSOP package.

Additional new LTC products featured in this issue include the LT1175, a negative low-dropout regulator. We have articles that detail several circuits for powering the Pentium™ microprocessor.

Also, we begin a series of articles on power-factor correction. We present Design Information on components for HDSL and on RS232 transceivers for DTE-DCE switching. Our Design Ideas section is, as usual, overflowing. LT

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LTC in the News

Linear Technology Reports Record Quarterly Sales, Increases Quarterly Dividend

Thanks to your support of Linear Technology's products, our sales reached a record $62.1 million for the second quarter of fiscal 1995, ended January 1, 1995—an increase of 29% over the same quarter last year. Net income for the quarter was $19.2 million, an increase of 47% over last year. A quarterly cash dividend of $0.07 was paid on February 15, 1995 to shareholders of record on January 27, 1995.

In its November 7th, 1994 issue, *Forbes* magazine again named Linear Technology one of its "Best 200 Small Public Companies in America." This marks the fifth year in a row that the Company has been included. This year Linear Technology ranked 97th, up from 102nd last year.

In a separate story in the same issue, entitled "Small Footprints, Big Impressions," *Forbes* pointed out that LTC is one of only two companies on the list to have a capitalized value greater than a billion dollars. Among 200 companies in the listing, LTC is 40th in sales growth, seventh in net income, and fifth in market value. All in all, a very impressive showing.

LTC received the Emerging Company Award for 1995 from the Silicon Valley Chapter of Association for Corporate Growth. LT

New LTC1266 Switching Regulator Provides High Efficiency at 10A Loads

by Greg Dittmer

Introduction

The new LTC1266 is a synchronous, stepdown switching-regulator controller that can drive two external, N-channel MOSFET switches. The superior performance of N-channel MOSFETs enables the LTC1266 to achieve high efficiency at loads of 10A or more with few additional components. Burst Mode™ operation provides high efficiency at light loads—efficiency is greater than 90% for loads from 10mA to 10A. The ability to provide 10A at high efficiency is critical for supplying power to Pentium™ applications.

The LTC1266 is based on the LTC1148 architecture, and has most of the features of this successful product, including constant off-time, current-mode architecture with automatic Burst Mode operation. As with the LTC1148, current-mode control provides excellent line and load transient response, inherent short-circuit protection, and controlled startup current with minimal voltage overshoot. Pin-selectable shutdown reduces the DC supply current to 40 microamps. The LTC1266 also has a pin-selectable phase option, which allows it to drive a P-channel top-side switch, instead of an N-channel, as in the case of the LTC1148.

Other new features of the LTC1266 not available in the LTC1148 include an on-chip low-battery comparator, pin-defeatable Burst Mode, a wider voltage supply range (3.5V to 20V), 1% load regulation, and a higher maximum frequency of 400kHz.

N-Channel versus P-Channel

The key to the LTC1266's ability to drive large loads at high efficiencies is its ability to drive both top-side and bottom-side N-channel MOSFETs. The rest of the LTC1148 family controllers require a P-channel MOSFET for the top-side switch. For load currents above about 5 amps, there are few P-channel MOSFETs available that can do the job at reasonable efficiencies.

The superiority of N-channel MOSFETs over P-channels is due to the lower $R_{DS(ON)}$ and lower gate capacitance achievable in the N-channel parts. The lower $R_{DS(ON)}$ results from the higher mobility of electrons, the majority carrier in N-channel devices, compared to holes, the majority carrier in P-channel devices. To compensate for the higher $R_{DS(ON)}$ of the P-channel, the channel width is usually made larger, resulting in higher gate capacitance. Efficiency is inversely proportional to both $R_{DS(ON)}$ and gate capacitance. Higher $R_{DS(ON)}$ decreases efficiency due to higher I^2R losses and limits the maximum current the MOSFET can handle without exceeding thermal limitations; higher gate capacitance increases losses due to the increased charge required to switch the MOSFETs on and off during each switching cycle. Even with these performance advantages, the N-channel MOSFETs are generally cheaper than P-channel.

Driving N-Channel MOSFETs

If N-channels are so superior to P-channels, why are the rest of the LTC1148 family of synchronous controllers designed to drive P-channels? The answer is that P-channels have a distinct advantage—simplicity of the gate drive. This is clear when comparing the waveforms in Figures 1a and 1b. Because of the negative threshold of the P-channel, the gate potential must decrease below the source (which is at V_{IN}) by at least $V_{GS(ON)}$ to turn it on. Hence, the top-side MOSFET can be gated between the available supply rail, V_{IN}, and ground.

On the other hand, driving an N-channel top-side MOSFET isn't so straightforward. When the top-side MOSFET is turned on, the source is pulled up to V_{IN}. Because the N-channel has a positive threshold voltage, the gate must be above the source by at least $V_{GS(ON)}$. Thus, the top-side drive must swing between ground

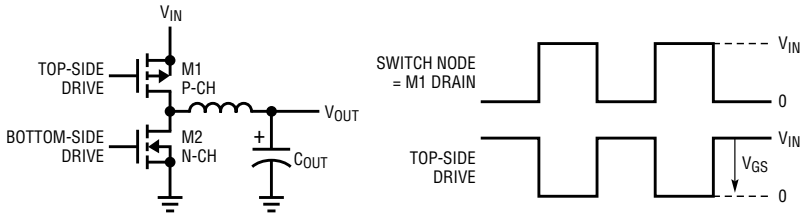


Figure 1a. Drive requirements for all N-channel MOSFET buck converter

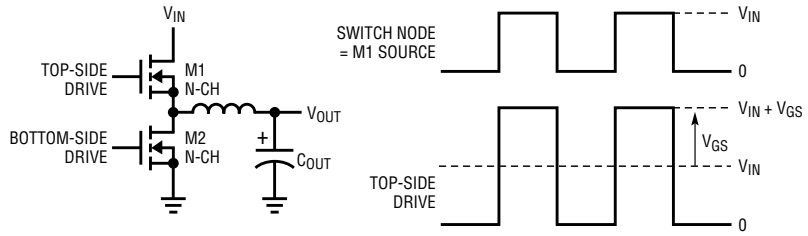


Figure 1b. Drive requirements for complementary MOSFET buck converter

Burst Mode is a trademark of Linear Technology Corporation.

and V_{IN} + $V_{GS(ON)}$. This requires a second, higher supply rail equal to at least V_{IN} + $V_{GS(ON)}$.

There are two ways to obtain this higher rail. The most straightforward way is if a higher rail is already available, as is the case in most desktop systems that have 12V supplies. This configuration is shown in Figure 2a. Note that the Power V_{IN} input to the LTC1266 is dedicated to powering the internal drivers and is separate from the main supply input. The Power V_{IN} voltage cannot exceed 18V (20V max), limiting the input voltage to

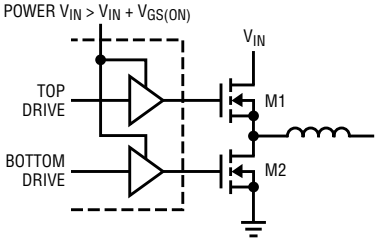


Figure 2a. Simplified schematic of all N-channel converter with additional supply voltage (Power V_{IN} > V_{IN} + $V_{GS(ON)}$)

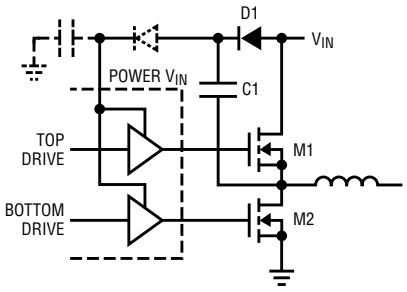


Figure 2b. Simplified schematic of all N-channel converter with charge pump

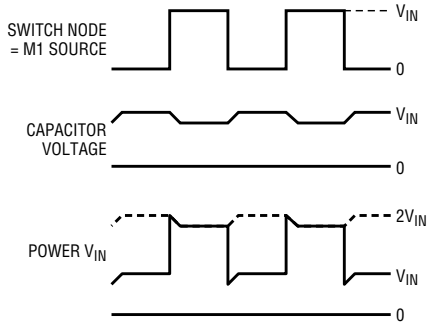


Figure 2c. Waveforms for charge pump circuit in Figure 2b

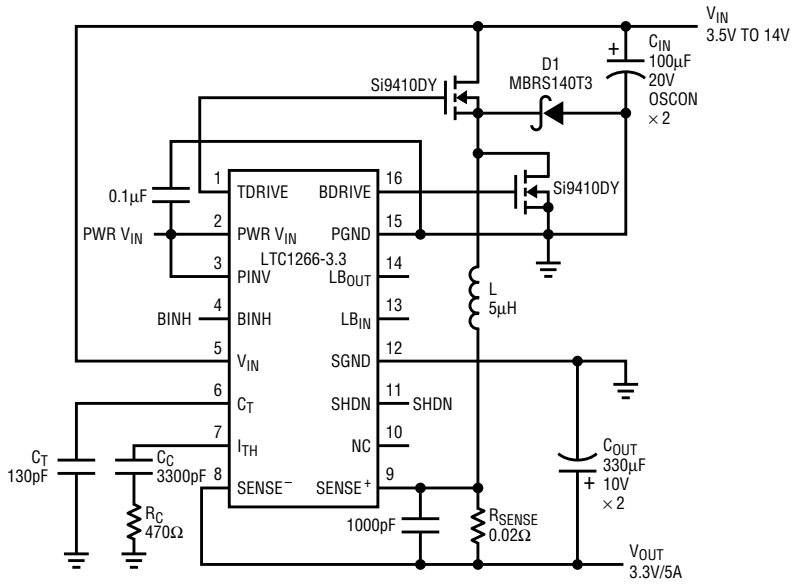


Figure 3a. All N-channel 3.3V/5A regulator with external power V_{IN}

18 – $V_{GS(ON)}$. For a converter with logic-level MOSFETs, this limits V_{IN} to about 14V. The Power V_{IN} voltage must also meet its minimum requirement of V_{IN} + $V_{GS(ON)}$ (about 10V for a 5V to 3.3V converter) in order not to burn up the high-side MOSFET due to insufficient conductance at larger output loads.

If this higher rail is not available, a charge-pump circuit can be used to pump V_{IN} to the required level, as shown in Figure 2b. During the off cycle, when M2 is on, capacitor C1 is charged to V_{IN} through D1. Power V_{IN} and the gate of the bottom-side MOSFET are therefore at V_{IN}. When the on-cycle commences, the internal driver places the charge-pump capacitor voltage across the gate-source of M1 and, as the source rises to V_{IN}, V_{GS} remains constant at V_{IN}. There will be a small reduction of V_{GS} as some charge is transferred from the charge-pump capacitor to the gate capacitance of M1, although, for a charge-pump capacitor of 0.1 microfarad or larger, this reduction is almost negligible. During the on cycle, the voltage at the LTC1266 Power V_{IN} pin rises to twice V_{IN}. Since the absolute maximum at this pin is 20V, this limits V_{IN} to 9V in this circuit configuration. A higher V_{IN} (about 13V) is allowable if C1 is charged from a fixed 5V source. For voltages above 13V, a P-channel top-side switch must be used, since in this configuration, the gate drive needs only to swing from V_{IN} to ground. Multiple P-channel MOSFETs may need to be paralleled, however, to meet the load requirements.

Figures 3, 4, and 5 show the three basic circuit configurations for the LTC1266. The all-N-channel, external Power V_{IN} circuit shown in Figure 3 is a 3.3V/5A surface-mount converter. The current-sense resistor value is chosen to set the maximum current to 5A, according to the formula I_{OUT} = 100mV/R_{SENSE}. With V_{IN}

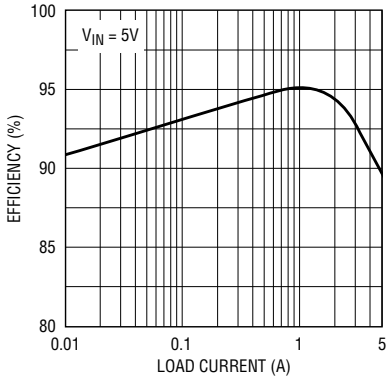


Figure 3b. Efficiency for Figure 3a's circuit

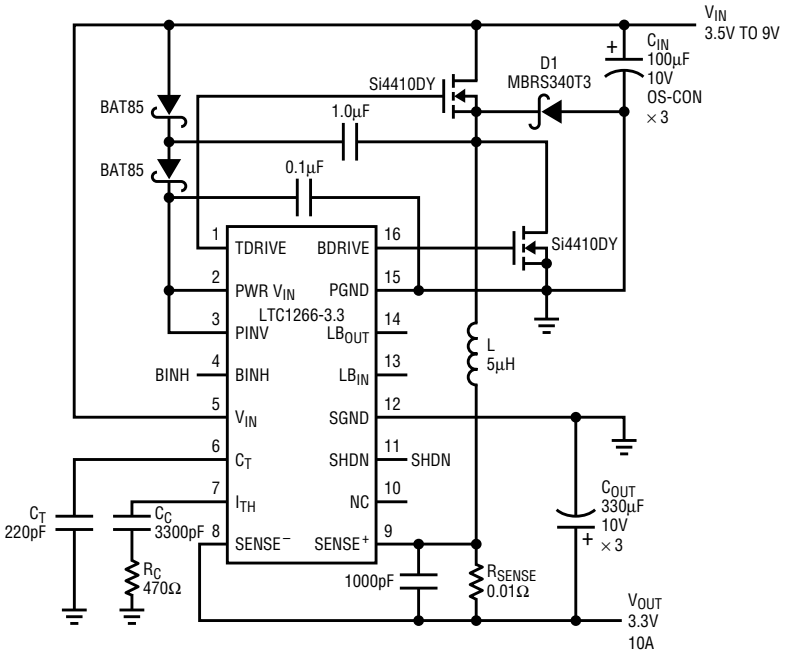


Figure 4a. All N-channel single-supply 5V to 3.3 V/10 amp regulator

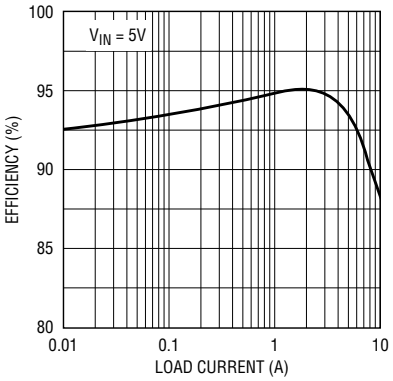


Figure 4b. Efficiency for Figure 4a's circuit

= 5V, the 5µH inductor and 130pF timing capacitor provide an operating frequency of 175kHz and a ripple current of 1.25A. The $V_{GS(ON)}$ of the Si9410 N-channel MOSFETs is 4.5V; thus the minimum allowable voltage at the external Power V_{IN} is V_{IN} MAX + 4.5V. At the other end, Power V_{IN} should be kept under the maximum safe level of 18V, limiting V_{IN} to 18V – 4.5V = 13.5V.

Figure 4 shows an LTC1266 in the charge-pump configuration designed to provide a 3.3V/10A output. The Si4410s are new logic-level, surface-mount, N-channel MOSFETs from Siliconix that provide a mere 20 milliohms of on-resistance at V_{GS} = 4.5V, and thus provide a 10A solution with minimal components. The efficiency plot shows that the converter still is close to 90% efficient at 10A. Because the charge-pump configuration is used, the maximum allowable V_{IN} is 18V/2 = 9V. See the LTC1266 data sheet for a charge-pump circuit that allows input voltages above 9V. Due to the high AC currents in this circuit, we recommend low ESR OS-CON input/output capacitors to maintain efficiency and stability.

Figure 5 shows the conventional P-channel, topside switch circuit configuration for implementing a 3.3V/3A regulator. The P-channel configuration allows the widest possible supply range of the three basic circuit configurations, 3.5V to 18V, and provides extremely low dropout, exceeding that of most linear regulators. The low dropout results from the LTC1266's ability to achieve a 100% duty cycle when in P-channel mode. In N-channel mode, the duty cycle is

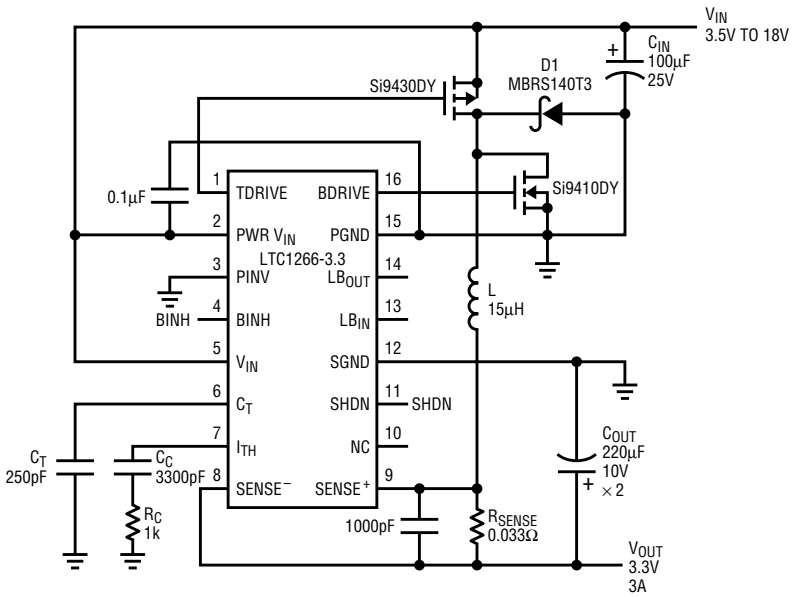


Figure 5a. Low-dropout 3.3V/3A complementary MOSFET regulator

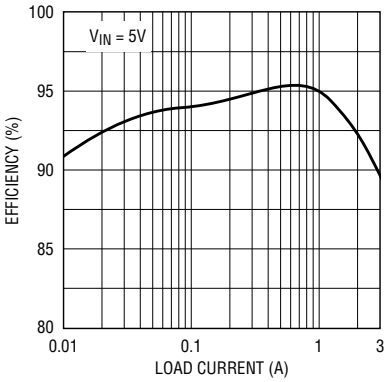


Figure 5b. Efficiency for Figure 5a's circuit

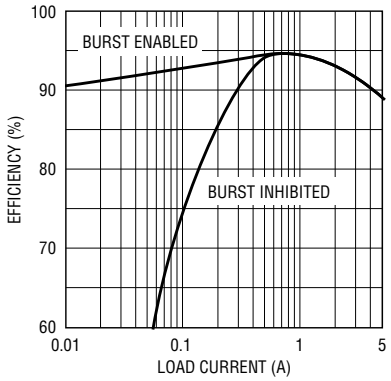


Figure 6. Efficiency comparison: Burst Mode enabled/disabled

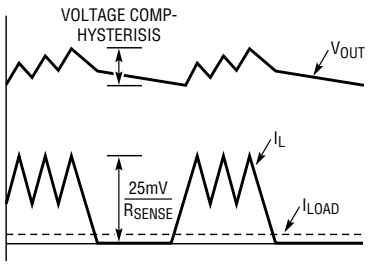


Figure 7a. Inductor current and output voltage waveforms: Burst Mode enabled

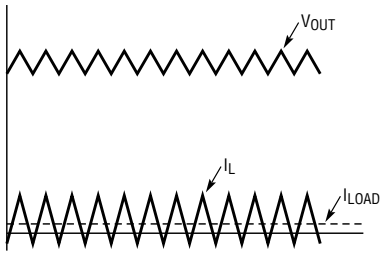


Figure 7b. Inductor current and output voltage waveforms: Burst Mode disabled

limited to less than 100% to ensure proper startup, and thus the dropout voltage for the all N-channel converters is slightly higher.

The three application circuits demonstrate the fixed 3.3V version of the LTC1266. The LTC1266 is also available in fixed 5.0V and adjustable versions. All three versions are available in 16-pin narrow SOIC and DIP packages.

Burst Mode Inhibit

The LTC1266 also provides a function to disable Burst Mode with a CMOS logic high applied to pin 4. When observing the performance of a regulator at light loads with and without Burst Mode (see Figure 6), the performance enhancement that Burst Mode offers is immediately obvious. So why disable Burst Mode? There are certain conditions when the disadvantages of Burst Mode outweigh the advantages, and it is useful to have an easy way to disable this feature. The most common reasons for disabling Burst Mode are: 1) at light loads, the long burst cycles cause operating frequencies in the audio range, causing audible noise; 2) Burst Mode puts certain restrictions on the maximum ESR of the output capacitor, since excessive ESR (relative to the sense resistor) may falsely trigger Burst Mode. If Burst Mode is disabled, this restriction can be relaxed, at the expense of efficiency; and 3) If the circuit uses auxiliary winding(s), which depend on continuous switching in the primary to transfer energy to the secondary, disabling Burst Mode guarantees this switching, independent of the primary load.

Figure 7 shows the difference between LTC1266 operation at light loads, with Burst Mode enabled and disabled. When Burst Mode is enabled (Figure 7a), the lower limit of the current-trip threshold ($25mV/R_{SENSE}$) prevents the current comparator from regulating a load below this value. The output will slowly rise until the hysteretic voltage comparator trips, at which time sleep mode commences. During sleep mode, both MOSFETs are turned off and the output capacitor supplies the load current until it discharges to the lower threshold of the voltage comparator. When this lower threshold is reached, the main loop turns on briefly again to recharge the capacitor.

When Burst Mode is disabled, the lower limit of the current trip threshold is allowed to go below zero (instead of $25mV/R_{SENSE}$). This allows the current comparator to regulate the output voltage down to zero load without having to rely on the voltage comparator for regulation. At zero load, the inductor-current waveform will be symmetrical around zero, so that the average current equals zero. During the negative current phase of the cycle, current is reversing, that is, flowing out of the output capacitor back through the inductor to ground or to the supply, in order to keep the average current zero. The voltage comparator is not required when Burst Mode is disabled; Therefore, to ensure that it doesn't interfere with the current comparator operation, the upper threshold is raised up to take it out of the picture; however, it is still present to prevent the output voltage from overshooting.

Low-Battery Comparator

The LTC1266 also includes a low-battery comparator. This comparator compares the voltage applied to pin 13 to an internal 1.25V reference and provides an open-drain output at pin 14. This 1.25V reference is dedicated to the low-battery comparator and is active even when the rest of the chip is shut down or nonfunctional due to low supply voltage. This comparator can operate down to a supply voltage of 2.5V, whereas the rest of the chip stops functioning at about 3.5V.

Conclusion

The new LTC1266 synchronous stepdown regulator controller is the first LTC synchronous controller with the ability to exploit the superior performance of N-channel MOSFETs to maximize efficiency and provide a low-cost, compact solution for converters. The extra features also provided in this product—Burst Mode inhibit and a low-battery comparator—make it ideal in a wide variety of applications.

The LTC1267 Dual Switching-Regulator Controller Operates from High Input Voltages

by Randy G. Flatness

Introduction

The LTC1267 dual switching regulator controller is the latest addition to Linear Technology's family of better than 90% efficient step-down DC/DC converters. The LTC1267 features an extremely wide, 4V-to-40V input operating-voltage range and reduced supply currents. The quiescent current is a low 250 microamps, and current in shutdown mode drops to less than 20 microamps. The combination of low supply currents and high input-voltage capability is ideal for battery-powered applications that require high-voltage AC wall adapters.

LTC offers two versions of the LTC1267, both in space-saving 28-pin SSOP packages. The LTC1267 provides fixed output voltages of 3.3V and 5V with individual shutdown capability. The adjustable LTC1267-ADJ provides two user-programmable output voltages, set by external resistive dividers.

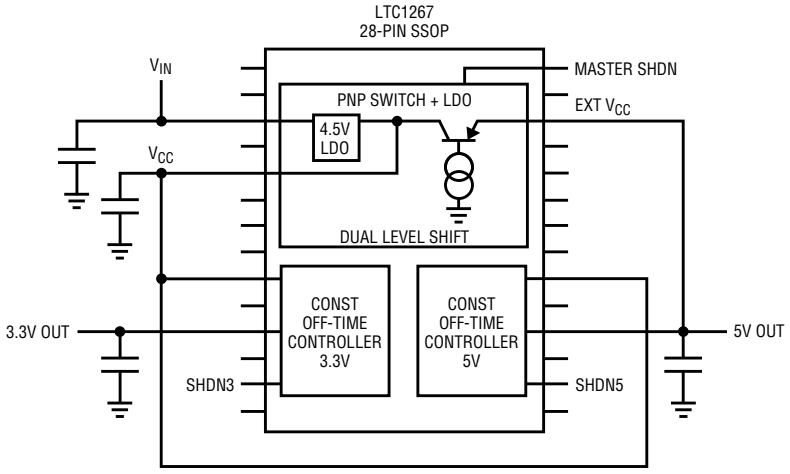


Figure 1. Simplified block diagram, LTC1267

High Efficiency with Dual Output Voltages

To boost efficiency, a unique EXT V_{CC} pin on the LTC1267 (also present on the single output LTC1159) allows the MOSFET drivers and control circuitry to be powered from an external source, such as the output of the regulator itself. Obtaining control and driver power from V_{OUT} improves efficiency at high input voltages, since the resulting current drawn from V_{IN} is scaled by the duty cycle of the regulator. During start-up and short-circuit conditions, operating power is supplied by an internal 4.5V low-dropout regulator. This regulator automatically turns off when the EXT V_{CC} pin rises above 4.5V. Figure 1 is a simplified block diagram of the control circuitry.

This 28-pin controller shares the same high performance, current-mode architecture and Burst Mode™

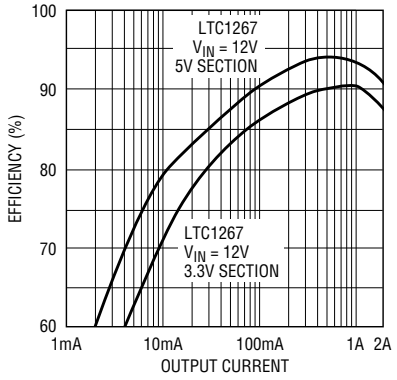


Figure 2. LTC1267 efficiency versus output current of Figure 3 circuit

Table 1. Dual-output switching-regulator controllers

	LTC1142	LTC1142HV	LTC1142HV-ADJ	LTC1143	LTC1267	LTC1267-ADJ
Minimum input voltage	4V	4V	4V	4V	5V	5V
Maximum input voltage (Abs Max)	16V	20V	20V	16V	40V	40V
Output voltage	3.3V & 5V	3.3V & 5V	(2) ADJ	3.3V & 5V	3.3V & 5V	(2) ADJ
Maximum switching frequency	250kHz	250kHz	250kHz	400kHz	400kHz	400kHz
MOSFET gate-drive voltage	V_{IN}	V_{IN}	V_{IN}	V_{IN}	EXT V_{CC}	EXT V_{CC}
Synchronous?	YES	YES	YES	NO	YES	YES
Package	28 SSOP	28 SSOP	28 SSOP	16 SOIC	28 SSOP	28 SSOP

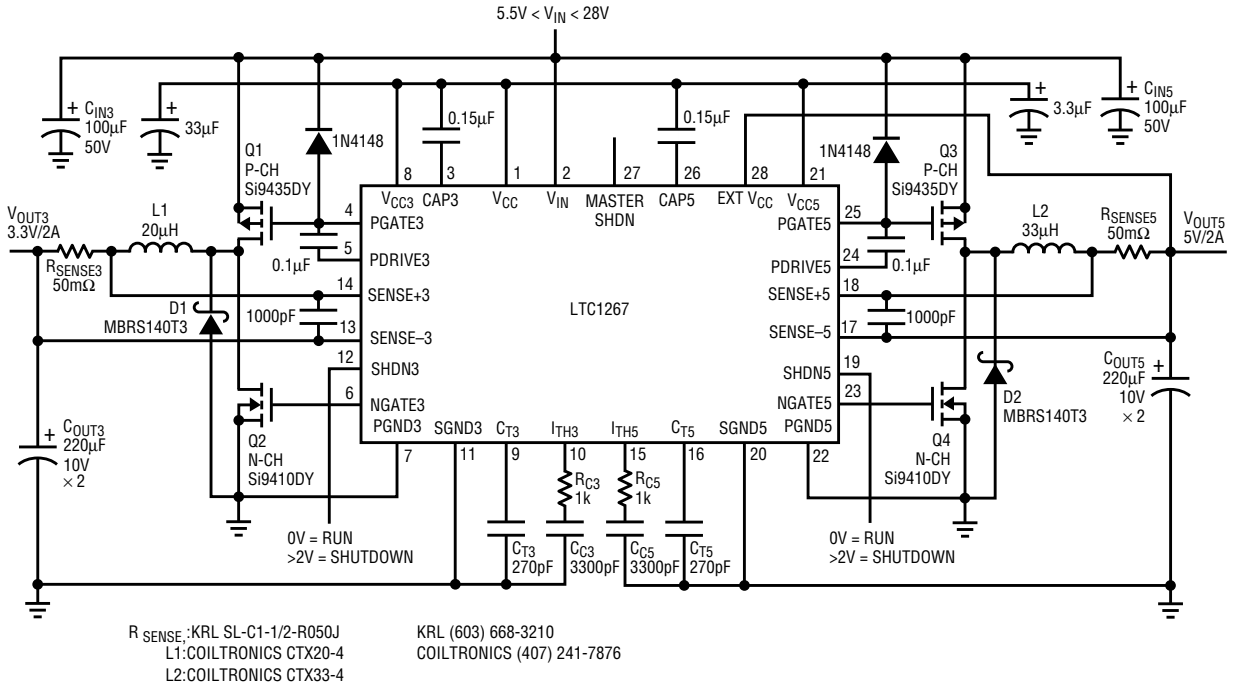


Figure 3. LTC1267 dual output 3.3V and 5V high-efficiency regulator

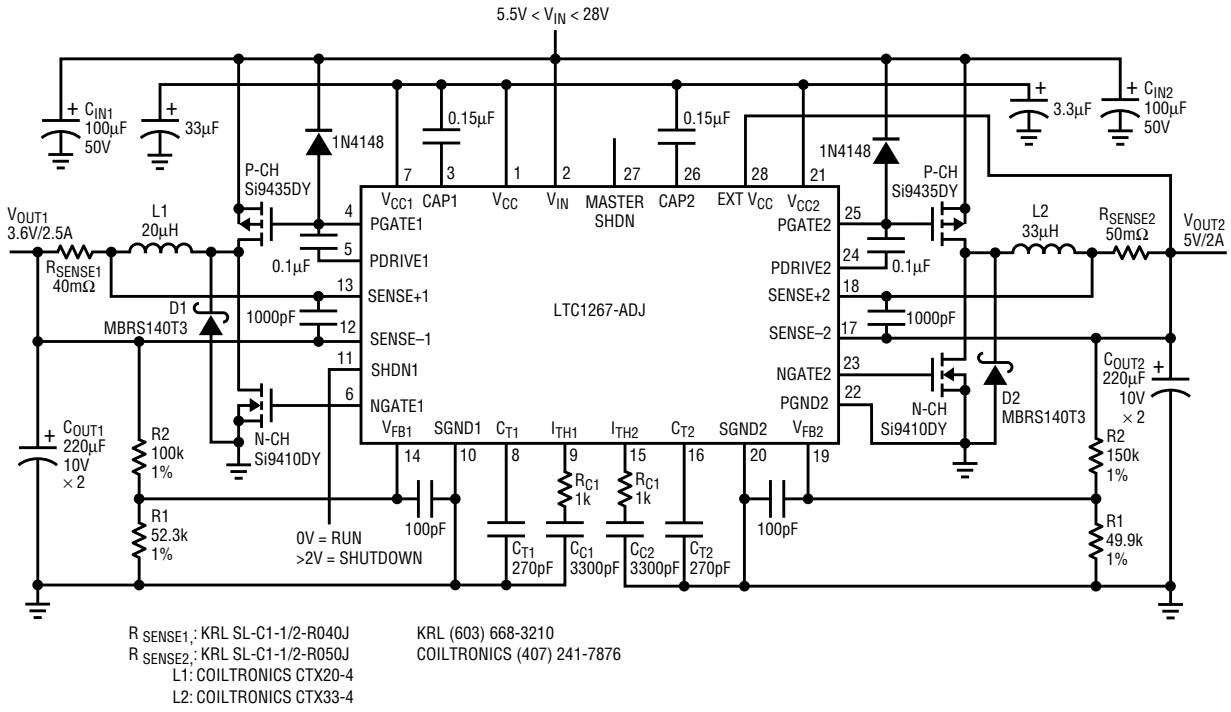


Figure 4. LTC1267 dual, adjustable, high-efficiency regulator circuit. Output voltages set at 3.6V and 5V

operation as the LTC1142HV (see the comparison in Table 1). The LTC1267 automatically switches to Burst Mode™ operation at low output currents to maintain greater than 90% efficiency over two decades of load current range. The wide operating range is illustrated by the typical efficiency curve of Figure 2. Battery life is extended by providing high efficiencies at load currents from a few milliamps (when the device is in standby or sleep modes) to Amps (under full power conditions).

pin for only one of its two outputs.

The higher input-voltage capability of the LTC1267 is required by battery-powered systems that use many cells in series to provide more power and longer battery life for high-performance portable systems. For 12-cell and larger applications, the AC adapter voltage can be as high as 30V, well below the 40V maximum of the LTC1267, allowing operation directly from the AC adapter. (If the application uses an AC adapter voltage of 18V or less, the dual output

All members of the LTC1142/LTC1267 family are capable of 100% duty cycle, providing very low dropout operation — lower than that of most linear low-dropout regulators — and all have built-in current limiting

Description

Both regulator blocks in the LTC1267 use a constant off-time current-mode architecture. This results in a power supply that has very high efficiency over a wide load current range, fast transient response, and very low dropout. The LTC1267 is ideal for applications that require 3.3V and 5V to be implemented with the highest conversion efficiencies over a wide load current range in a small board space. The LTC1267-ADJ has two externally adjustable outputs, which allow remote load sensing and user-customized output voltages.

Each regulator section employs a pair of external, complementary MOSFETs and a user-programmable current sense resistor for setting the operating current level to optimize performance for each application. A master shutdown pin turns off both main outputs and the 4.5V LDO. Both outputs in the LTC1267 have individual shutdown capability, whereas the LTC1267-ADJ has a shutdown

LTC1142HV or LTC1142HV-ADJ can be used.) At low input voltages, the internal 4.5V low-dropout regulator stays in regulation with only a 5V input voltage, extracting the maximum possible energy from the battery pack.

All members of the LTC1142/LTC1267 family are capable of 100% duty cycle, providing very low dropout operation (lower than that of most linear low-dropout regulators), and all have built-in current limiting. As the input voltage on the LTC1267 drops, the loop extends the on-time for the P-channel switch (off-time is constant), thereby keeping the inductor ripple current constant. Eventually the on-time extends so far that the P-channel MOSFET is on at DC or 100% duty cycle. Load and line regulation are excellent for a wide variety of conditions, including making the transition from Burst Mode™ operation to continuous-mode operation.

Typical Applications

Fixed Output 3.3V and 5V Converter

A fixed LTC1267 application circuit creating 3.3V/2A and 5V/2A is shown in Figure 3. The operating efficiency, shown in Figure 2, exceeds 90% for both the 3.3V and 5V sections. The 3.3V section of the circuit in Figure 3 comprises the main switch Q1, synchronous switch Q2, inductor L1, and current shunt R_{SENSE3}.

The 5V section is similar and comprises Q3, Q4, L2, and R_{SENSE5}. Each current-sense resistor (R_{SENSE}) monitors the inductor current and is used to set the output current according to the formula $I_{OUT} = 100mV/R_{SENSE}$. Advantages of current control include excellent line and load transient rejection, inherent short-circuit protection, and controlled startup currents. Peak inductor currents for L1 and L2 are limited to 150mV/R_{SENSE} or 3.0A. The EXT V_{CC} pin is connected to the 5V output, increasing efficiency at high input voltages. The maximum input voltage is limited by the MOSFETs and should not exceed 28V.

Adjustable Output 3.6V and 5V Converter

The adjustable output LTC1267-ADJ shown in Figure 4 is configured as a 3.6V/2.5A and 5V/2A converter. The resistor divider composed of R1 and R2 sets the output voltage according to the formula $V_{OUT} = 1.25V (1 + R2/R1)$. The input voltage range for this application is 5.5V to 28V.

Conclusion

The LTC1267 adds even more versatility to Linear Technology's family of high-efficiency step-down regulator controllers. Providing for up to 40V input voltage, the LTC1267 allows the use of higher voltage wall adapters. The 28-pin SSOP package and associated external components make dual output voltage, high-efficiency DC-to-DC conversion feasible in the extremely small board space available in today's portable electronics.

The LTC1265: a New, High-Efficiency Monolithic Buck Converter

by San-Hwa Chee

Introduction

The LTC1265 is a 14-pin SOIC stepdown converter (also available in a DIP package), capable of operating at frequencies up to 700kHz. High-frequency operation permits the use of a small inductor for size-sensitive applications. The LTC1265 has an internal 0.3Ω (at a supply voltage of 10V) P-channel power MOSFET switch, which is capable of supplying up to 1.2A of output current. With no load, the converter requires only 160µA of quiescent current; this decreases to a mere 5µA in shutdown conditions. In dropout mode, the internal P-channel power MOSFET switch is turned on continuously (at DC), thereby maximizing the life of the battery source. The part is protected from output shorts by its built-in current limiting. In addition to the features already mentioned, the LTC1265 incorporates a low-battery detector.

The LTC1265 uses a constant off-time, current-mode architecture. This results in a power supply that has very high efficiency over a wide load-current range

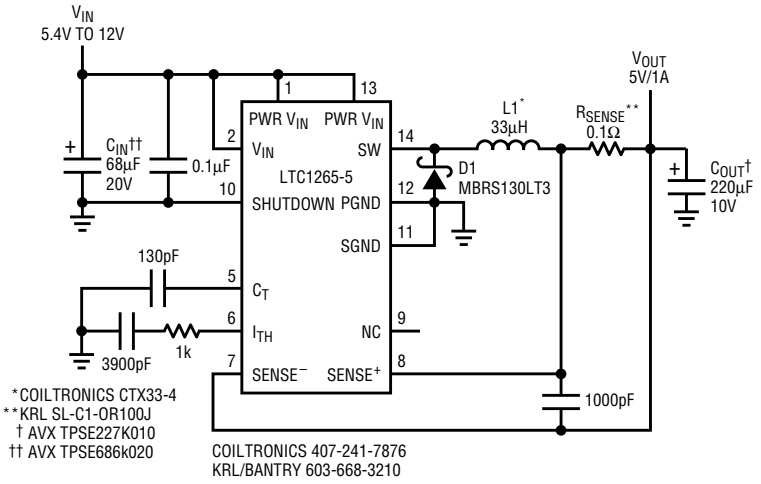


Figure 1. High-efficiency step-down converter

The LTC1265, like the LTC1147, is a current-mode DC-to-DC converter with Burst Mode™ operation. The current-mode architecture gives the LTC1265 excellent load and line regulation. Burst Mode results in high efficiency with both high and low load currents. The LTC1265 comes in three versions: the LTC1265-5 (5V output), the LTC1265-3.3 (3.3V output), and the LTC1265 (adjustable). All versions operate down to an input voltage of 3.5V and up to an absolute maximum of 13.5V.

Efficiency

Figure 1 shows a typical LTC1265-5 application circuit. The efficiency curves for two different input voltages are shown in Figure 2. Note that the efficiency for a 6V input exceeds 90% over a load range from less than 10mA to 850mA. This makes the LTC1265 attractive for all battery operated products and efficiency-sensitive applications.

High-Frequency Operation

Although the LTC1265 is capable of operating at frequencies up to 700kHz, the highest efficiency is achieved at an operating frequency of about 200kHz. As the frequency increases, losses due to the gate charge of the P-channel power MOSFET increase (see Figure 3). In space-sensitive applications, high frequency operation allows the use of smaller components at the cost of four to five efficiency points.

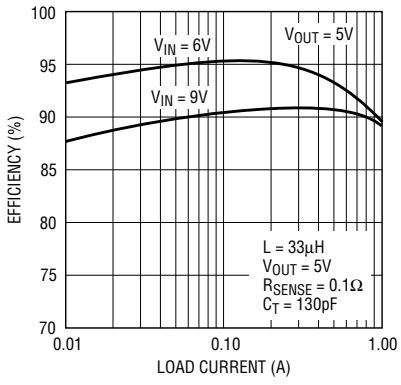


Figure 2. Efficiency versus load current

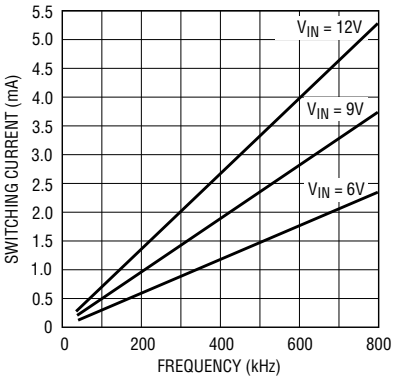


Figure 3. Gate charge losses versus frequency

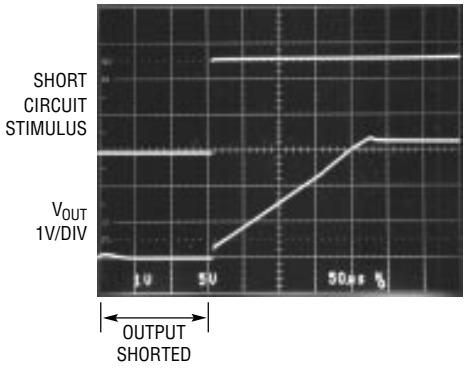


Figure 4. Short-circuit and start-up response of the LTC1265

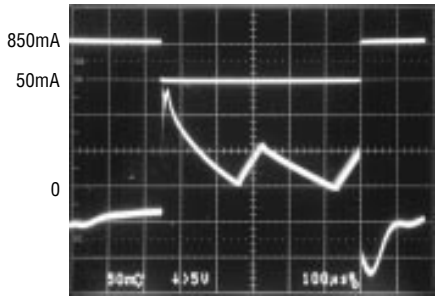


Figure 5. Load transient response

Constant Off-Time Architecture

The LTC1265 uses a constant off-time, current-mode architecture. This results in a power supply that has very high efficiency over a wide load-current range, fast transient response, and very low dropout characteristics. The off-time is set by an external capacitor, and is constant whenever the output is in regulation. When the output is not in regulation, the off-time is inversely proportional to the output voltage. By using a constant off-time scheme, the inductor's ripple current is predictable and well controlled under all operating conditions, making the selection of the inductor much easier. The inductor's peak-to-peak ripple current is inversely proportional to the inductance in continuous mode. If a lower ripple current is desired, a larger inductor can be used for a given value of external capacitor.

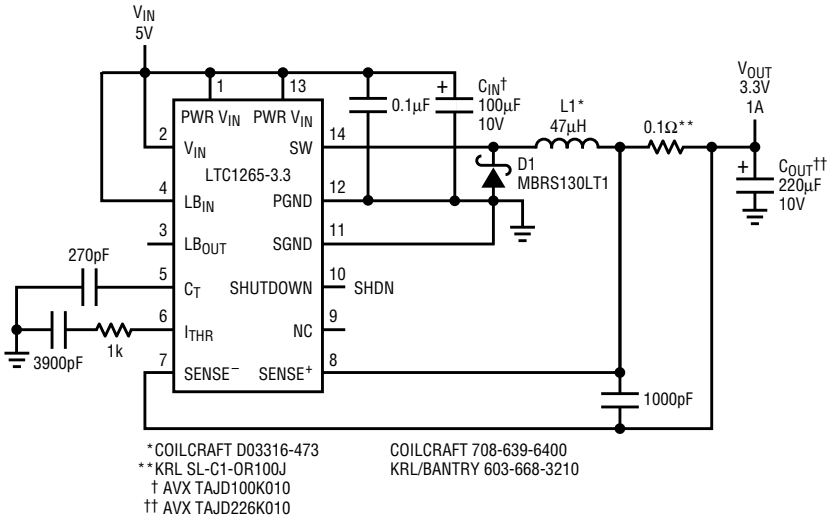


Figure 6. High-efficiency 5V to 3.3V converter

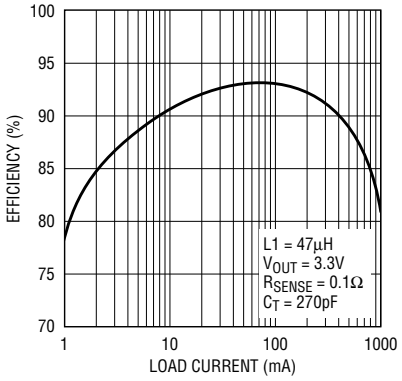


Figure 7. Efficiency versus load current

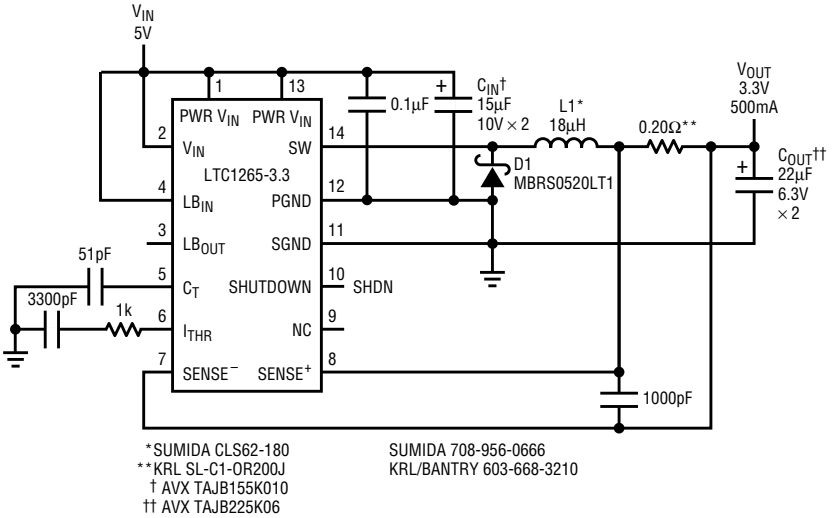


Figure 8. 2.5mm-high, 5V-to-3.3V converter (500mA output current)

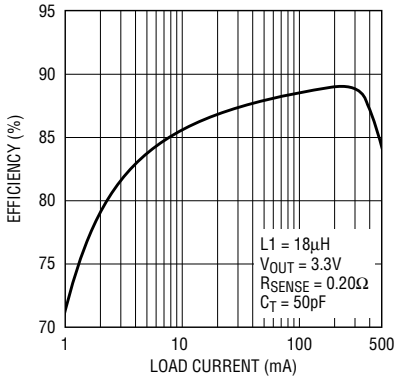


Figure 9. Efficiency versus load current

100% Duty Cycle in Dropout Mode

When the input voltage decreases, the switching frequency decreases. With the off-time constant, the on-time is increased to maintain the same peak-to-peak ripple current in the inductor. When the input-to-output voltage differential drops below 1.5V, the off-time is reduced. This prevents the operating frequency from dropping below 20kHz as the regulator approaches dropout. As the input voltage drops further, the P-channel switch is turned on for 100% of the cycle. The dropout voltage is governed by the switch resistance, load current, and current-sense resistor.

Good Start-Up and Transient Behavior

The LTC1265 exhibits excellent start-up behavior when it is initially powered-on or recovering from a short circuit. This is achieved by making the off-time inversely proportional to the output voltage when the output is still in the process of reaching its regulated value. When the output is shorted to ground, the off-time is extended long enough to prevent inductor current run-away. When the short is removed, the output capacitor begins to charge and the off-time gradually decreases. Note the absence of overshoot when the output comes out of a short-circuit, as shown in Figure 4. The initial power-up waveform is similar.

In addition, the LTC1265 has excellent load-transient response. When the load current drops suddenly, the feedback loop responds quickly by turning off the internal P-channel switch. Sudden increases in output current will be met initially by the output capacitor, causing the output voltage to drop slightly. Tight control of the inductor's current, as mentioned above, means that output-voltage overshoot is virtually eliminated (see Figure 5).

Typical Applications

5V-to-3.3V Converter

Figure 6 shows the LTC1265 configured for 3.3V output with 1A output-current capability. This circuit operates at a frequency of 100kHz. Figure 7 is the efficiency plot of the circuit. At a load current of 100mA, the efficiency is at 92%; the efficiency falls to 82% at a 1A output.

2.5mm Typical-Height 5V-to-3.3V Regulator

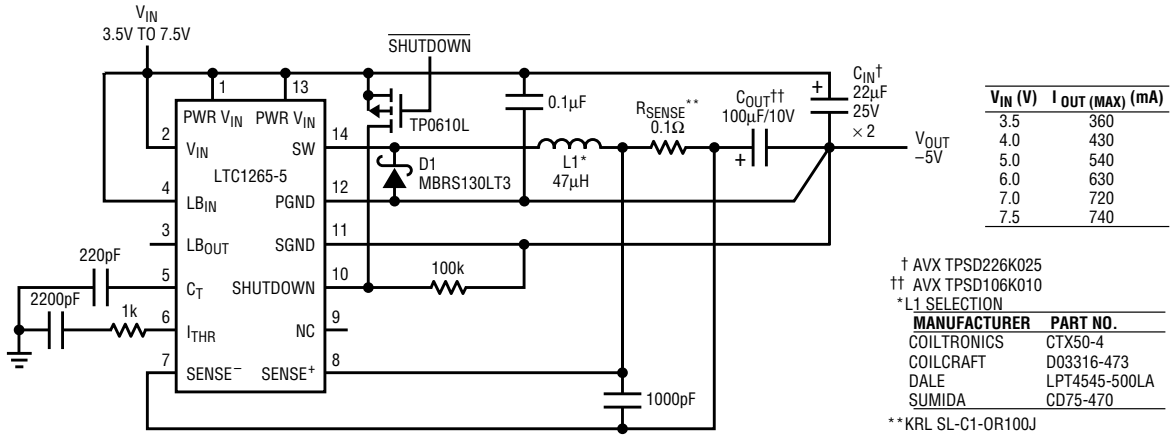
Figure 8 shows the schematic for a very thin 5V-to-3.3V converter. For the LTC1265 to be able to source 500mA output current and yet meet the height requirement, a small-value inductor must be used. The circuit operates at a high frequency (500kHz typically), increasing the gate charge losses. Figure 9 is the efficiency curve for this application.

Positive-to-Negative Converter

Besides converting from a positive input to positive output, the LTC1265 can be configured to perform a positive-to-negative conversion. Figure 10 shows the schematic for this application.

Conclusion

The LTC1265, with its low dropout and high efficiency, is ideal for battery-operated products and efficiency-sensitive applications. In addition, its ability to operate at high frequencies allows the use of small inductors for size-sensitive applications. LT



VIN (V)	I OUT (MAX) (mA)
3.5	360
4.0	430
5.0	540
6.0	630
7.0	720
7.5	740

† AVX TPSD226K025
†† AVX TPSD106K010
*L1 SELECTION

MANUFACTURER	PART NO.
COILTRONICS	CTX50-4
COILCRAFT	D03316-473
DALE	LPT4545-500LA
SUMIDA	CD75-470

**KRL SL-C1-OR100J

Figure 10. Positive (+3.5 to 7.5V) to negative (–5V) converter

The LT1175: Negative, Low-Dropout Regulator Complements LT1121/LT1129 Series

by Carl Nelson

Introduction

The LT1175 is a micropower, negative, low-dropout regulator that can supply up to 500mA load current. It is intended for regulating negative voltages between –3.8V and –20V, with input voltages up to –30V. Several new design techniques make the LT1175 easy to use and very tolerant of variations in the quality and size of the output capacitor. A low-dropout configuration, using an NPN pass transistor, gives the LT1175 the linear dropout characteristics of a large area FET design but with much smaller die area.

Figure 1a shows the basic configuration of the LT1175. In addition to the three terminals needed for a simple regulator, it has an output Sense pin, a Shutdown pin, and two current-limit-set pins (I_{LIM}). The total pin count is seven, allowing two pins on the 8-pin SO or DIP packages to be connected internally to the die-attach paddle. This gives much lower thermal resistance, allowing higher power dissipation in the regulator. For even higher power dissipation, the LT1175 is available in the 5-pin, surface-mount TO-220 package. The adjustable version of the part is shown in Figure 1b. Both I_{LIM} pins are internally connected to the input pin when the 5-pin package is used.

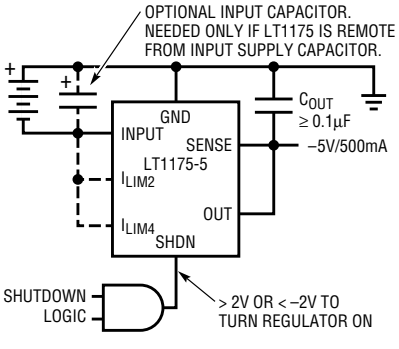


Figure 1a. Typical LT1175 circuit

In the adjustable version, the Sense pin allows custom selection of output voltage, with an external divider set to generate 3.8V at the Sense pin. The fixed 5V version uses the Sense pin to give true Kelvin connections to the load or to drive an external pass transistor for higher output currents. A separate Sense pin also allows for a new loop compensation technique described in more detail later.

Shutdown

The Shutdown pin is especially configured to be driven from either positive-voltage logic or with negative-only logic. Forcing the Shutdown pin two volts either above or below the ground pin will turn the regulator "on." This makes it simple to connect directly to positive logic signals for active-low shutdown. If no positive voltages are available, the Shutdown pin can be driven below the ground pin to turn the regulator "on." When left open, the Shutdown pin will default low to a regulator "on" condition. For all voltages below the absolute maximum ratings, the shutdown pin draws only a few microamperes of current.

In shutdown conditions, the LT1175 draws only about 10 microamps. Special circuitry is used to minimize increases in shutdown current at high temperatures, but a slight increase is seen above 125°C. One option not taken was to actively pull down on the output during shutdown. This is normally a good thing when the regulator is used by itself, but it prevents the user from shutting down the regulator when a second source of output power is connected to the LT1175 output. If active output pulldown is needed in shutdown conditions, this can be added externally with a few simple components.

Better Anti-Saturation

The NPN bipolar pass transistor used in the LT1175 gives small die area with low saturation resistance, but without precautions, this could cause quiescent supply current to be very high under certain conditions. When the regulator input voltage is too low to maintain a regulated output, the pass transistor is driven hard by the error amplifier as it tries to maintain regulation. The current drawn by the driver transistor (Q2 in Figure 3) could be tens of milliamperes with little or no load on the output. This was the case for older IC designs that did not actively limit driver current when the power transistor saturated. The LT1175 uses a new anti-saturation technique that prevents high driver current, yet allows the power transistor to approach its theoretical saturation limit. Using parallel feedback to the base of the driver and the error amplifier controls operating points for the anti-saturation circuitry much more precisely and achieves good loop stability. Very little increase in quiescent current is seen as the regulator enters the dropout condition.

Figures 2a and 2b, respectively, show the dropout and quiescent-operating-current characteristics of the LT1175. Note that the new anti-saturation circuitry keeps the dropout

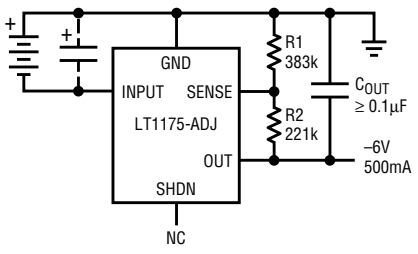


Figure 1b. Higher power LT1175 circuit: Adjustable LT1175 is available in TO-220 package

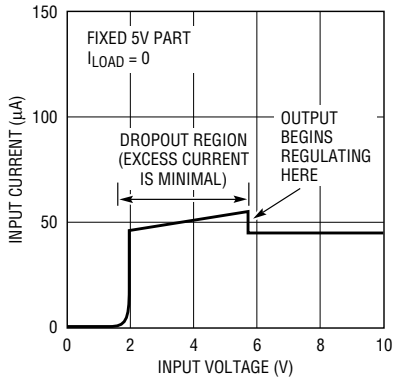


Figure 2a. LT1175 dropout characteristics

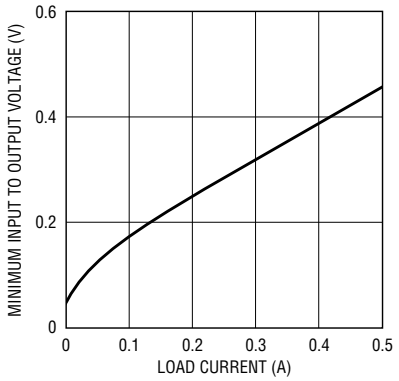


Figure 2b. LT1175 quiescent operating current

characteristics close to the optimal resistive shape, with very little excess quiescent current in dropout conditions.

Current Limit

The LT1175 uses two I_{LIM} pins to set the current limit at 200, 400, 600, or 800mA. This allows users to select current limits tailored to specific applications. Fixed-current-limit designs often result in short circuit currents three to ten times higher than full load current, and this can create problems with input overload or excessive power dissipation in a faulted load. Current limit is 200mA with both I_{LIM} pins floating. I_{LIM2} adds 200mA of available current and I_{LIM4} adds 400mA. The LT1175 is guaranteed to be "blowout proof," regardless of the current-limit setting. Internal power limiting (also known as foldback current limiting) and thermal shutdown protect the device from destructive junction temperatures.

An Improved Feedback Loop

Several new regulator design techniques make the LT1175 extremely tolerant of output capacitor variations. Like most low-dropout designs, which use a collector or drain of the power transistor to drive the output node, the LT1175 uses the output capacitor as part of the overall loop compensation. This generally requires the output capacitor to have a minimum value of 1–100µF, a maximum ESR (effective series resistance) of 0.1–1Ω, and a minimum ESR in the range of 0.03–0.3Ω. These restrictions usually could be met only with good-quality solid-tantalum capacitors. Aluminum capacitors have problems with high ESR unless much higher values of capacitance (physically large capacitors) are used. Ceramic or film capacitors have too low an ESR, which makes the capacitance/ESR zero frequency too high to maintain phase margin in the regulator. Even with optimum capacitors, loop-phase margin was very low in previous designs when output current was low. These problems led to a new design technique for the LT1175 error amplifier and internal frequency compensation, as shown in Figure 3.

A conventional regulator loop consists of error amplifier A1, driver transistor Q2, and power transistor Q1. Added to this basic loop are secondary loops generated by Q3 and C_F. A DC negative feedback current fed into the error amplifier through Q3 and R_N results in very low overall loop gain at light load currents. This is not a problem because very little gain is needed at light loads. The combination of low gain at light loads and the DC feedback moves the parasitic pole frequency at Q2's base out in frequency. The combination of these two effects dramatically improves loop phase margin at light loads, and makes the loop tolerate large ESR in the output capacitor. With heavy loads, loop phase and gain are not nearly as troublesome, and the negative feedback could degrade regulation. The logarithmic behavior of the base-emitter voltage of Q1 reduces Q3's negative feedback at heavy loads to prevent poor regulation.

In a conventional design, even with the nonlinear feedback, poor loop phase margin would occur at medium to heavy loads if the ESR of the output capacitor fell below 0.3Ω. This condition can occur with ceramic or film capacitors, which often have ESRs under 0.1Ω. The user is forced to add a resistor in series with the capacitor to guarantee loop stability. The LT1175 uses a unique AC feedforward technique to eliminate this problem. C_F is a conventional feedforward capacitor, often used in regulators to cancel the pole formed by the output capacitor. It would normally be connected from the regulated output node to feedback node at the R1–R2 junction, or to an internal node on the amplifier, as shown in Figure 3. In this case, however, it is connected to the internal structure of the power transistor. RC is the unavoidable parasitic collector resistance of the power transistor. Access to the node at the bottom of RC is available only in monolithic structures, where Kelvin connections can be made to the NPN buried-collector layer. The loop now responds as if RC were in series with the output capacitor, and good loop stability is achieved

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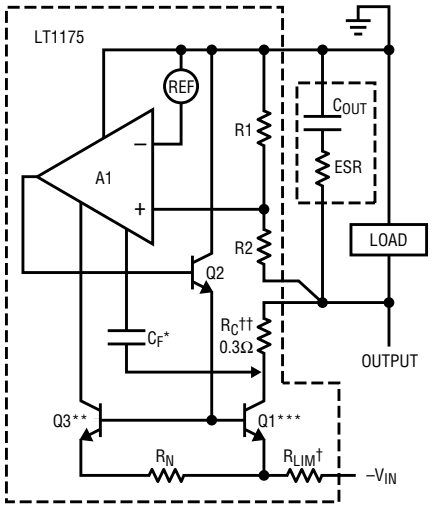


Figure 3. Block diagram of LT1175 illustrating new design techniques for internal frequency compensation and the error amplifier designs

The LTC1451, LTC1452, and LTC1453: 12-Bit, Rail-to-Rail, Micropower DACs in SO-8 Packages

by Hassan Malik
and Jim Brubaker

Flexible, Micropower DACs Offer True Rail-to-Rail Performance

The LTC1451, LTC1452, and LTC1453 are complete 12-bit, single-supply, rail-to-rail, voltage-output digital-to-analog converters. They include an output buffer amplifier and a Serial-Peripheral Interface (SPI) compatible, three-wire serial interface; a data-output pin makes daisy chaining possible. These DACs are guaranteed to have a DNL error of less than 0.5LSB. The typical DNL error is about 0.2LSB. A built-in power-on reset clears the output to zero scale. The output amplifier can swing to within 5 millivolts of V_{CC} when unloaded and can source or sink 5mA at a 4.5V supply. These DACs come in 8-pin PDIP and SO-8 packages.

The LTC1451 has an onboard reference of 2.048V and a nominal output swing of 4.095V. It operates from a single 4.5V to 5.5V supply dissipating 2mW (I_{CC} typical = 400µA).

The LTC1452 is a multiplying DAC with no onboard reference and a full-scale output of twice the reference input. It operates from a single supply that can range from 2.7V to 5.5V. It dissipates 1.125 mW (I_{CC} typical = 225µA) at a 5V supply and a mere 0.5mW (I_{CC} typical = 160µA) at a 3V supply.

The LTC1453 has a 1.22V onboard reference and a convenient full scale of 2.5V. It can operate on a single supply with a wide range of 2.7V to 5.5V. It dissipates 0.75mW (I_{CC} typical = 250µA) with a 3V supply.

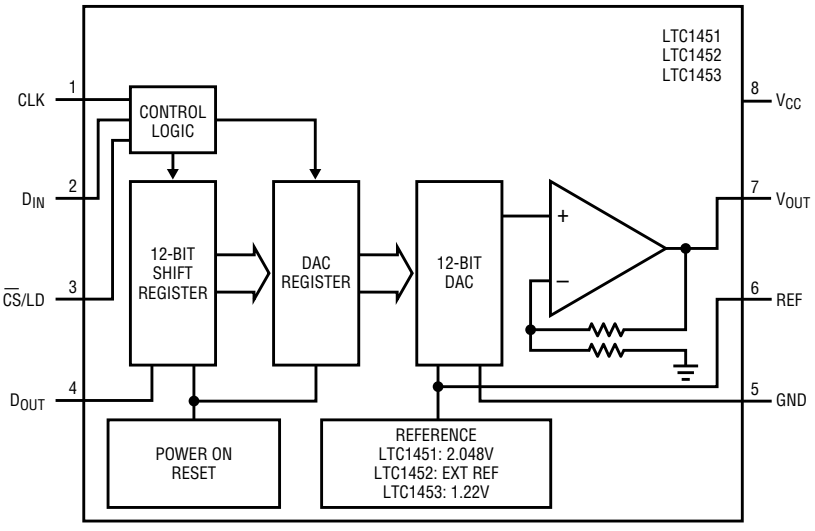


Figure 1. Block diagram, LTC1451 family

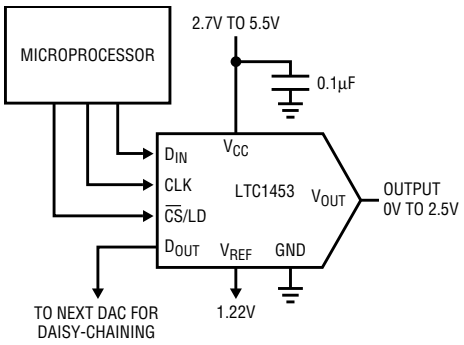


Figure 2. The 3V LTC1453 is SPI compatible and communicates with both 5V and 3V processors

Circuit Topology

Easy-to-Use, Space-Saving Serial I/O

Figure 1 shows a block and pin diagram of the LTC1451. The three digital inputs, CLK, DIN, and $\overline{CS}$/LD are TTL-level compatible. Data is shifted into the input shift register, MSB first, on the rising edge of CLK. When $\overline{CS}$/LD is high, the DAC registers are loaded from the shift register and the CLK is disabled internally to prevent noise. Data is latched in the DAC registers on the falling edge of $\overline{CS}$/LD, and is shifted out MSB first through the D_{OUT} pin. Multiple DACs can be daisy chained by connecting the D_{OUT} pin of one DAC to the DIN pin of the next. The digital inputs can swing to 5V, even when the DAC's V_{CC} is at 3V. This allows more flexibility when interfacing to the DAC. Figure 2 shows how these DACs are typically used with a 3V or 5V supply.

Patented Architecture Guarantees Excellent DNL

Figure 3 shows a block diagram of the DAC core. The LTC1451 family uses a proprietary architecture first used in the LTC1257 and described in more detail in Volume III, Number 3 of *Linear Technology*. In this architecture, the MSBs are decoded using a resistor ladder and the LSBs are decoded using a proprietary amplifier input stage. It requires no laser trimming and is inherently monotonic, with a typical DNL error of 0.2LSB.

Rail-to-Rail Output

The output amplifier is connected in a gain-of-two configuration, which means that the output at full scale is twice the reference voltage connected to the resistor ladder. The references on both the LTC1451 and LTC1453 can be overdriven to a higher voltage to increase the full-scale output. The opamp can swing to within 5mV of V_{CC} when unloaded, giving these rail-to-rail DACs an exceptional output-swing capability. The op amp can source or sink 5mA, even at a 4.5V supply, and has an output impedance of 50Ω when swinging to the rails. It has a wide input common-mode range that extends from ground to V_{CC} – 1.5V. The output glitch at midscale is 20nV-s and the digital feedthrough is a negligible 0.15nV-s.

A Wide Range of Applications

Some of the applications for this family include digital calibration, industrial process control, automatic test equipment, cellular telephones, and portable, battery-powered applications, where low supply current is essential.

Loop-Powered 4–20mA Process Controller

Figure 4 shows how to use an LTC1453 to make an opto-isolated digitally controlled 4–20mA process controller. The controller circuitry, including the opto-isolation, is powered by the loop voltage, which can have a wide range of 3.3V to 30V. The 1.22V reference output of the LTC1453 is used for the 4mA offset current and V_{OUT} is used for the digitally controlled 0–16mA current. R_S is a sense resistor and the op amp modulates the transistor Q1 to provide the 4–20mA current through this resistor. The potentiometers allow for offset and full-scale adjustment. The control circuitry dissipates well under the 4mA budget at zero scale.

Conclusions

The LTC1451, LTC1452, and LTC1453 are the most flexible, micropower, stand-alone DACs that offer true rail-to-rail performance. This flexibility, along with the tiny SO-8 package, allows these parts to be used in a wide range of applications where size, power, DNL, and single-supply operation are important.

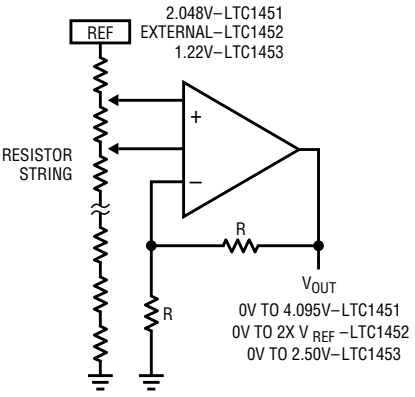


Figure 3. Proprietary op amp input stage ensures excellent DNL

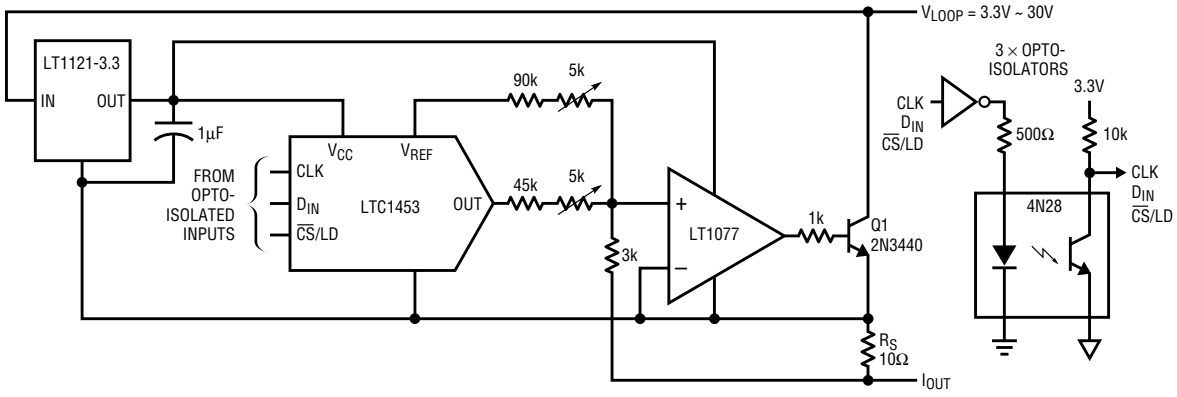


Figure 4. Opto-isolated 4–20 milliamp process controller

Power Factor Correction: Part I

by Dale Eagar

Introduction

The term "power-factor correction" (PFC) refers to the reduction of the harmonic content, and/or the aligning of the phase angle of incoming current so that it is in phase with the line voltage required to operate an electronic device. PFC is considered very beneficial to the environment because it makes more efficient use of existing power plants. PFC is subject to legislation and policy making throughout the industrialized world.

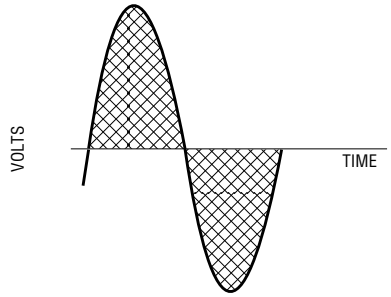


Figure 1a. Input line voltage

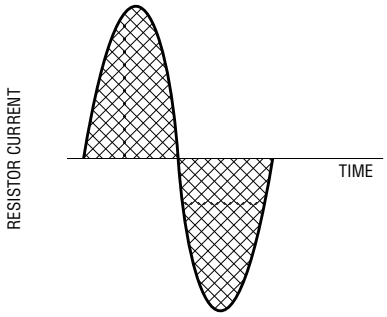


Figure 1b. Current drawn by a pure resistive load

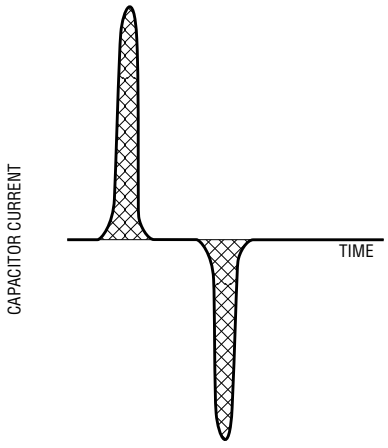


Figure 1c. Current drawn by a capacitive-input power supply

The European standard (IEC 555) sets maximum permissible values for the harmonics of the input line current that may be produced by equipment meeting these standards. By 1996, TV sets and other consumer equipment will be required to incorporate PFC. The benefit of PFC is realized as energy savings seen throughout the power distribution system. With PFC implemented throughout the industry, fewer new power plants will need to be built to meet projected energy demands. Consumers will pay more for "poor power factor" power at the power meter; it is hoped that, as a result, they will choose the beneficial "green" or PFC-equipped devices to save energy dollars.

Equipment that uses DC voltages derived from the AC line generally have a poor power factor because of the capacitive input to the DC power section. The waveforms in Figure 1 show the "evils" of capacitor input power supplies. Figure 1a represents the input line voltage; Figure 1b represents a "nice" waveform of current as drawn by a resistive load; Figure 1c represents the harmonic-rich current waveform drawn by a capacitive-input power supply.

How PFC Performs Its Magic

The trick behind PFC is simple: make the input look as much like a resistor as possible. Resistors have the perfect power factor (unity). From the power utility company's viewpoint, unity power factor is the load of choice, a load that allows their power distribution system to operate at its maximum efficiency.

Emulating a Resistor

A resistor is emulated at the input port of a PFC by loading the incoming power line with a programmable current sink that is programmed with a voltage proportional to the instantaneous line voltage (Figure 2a.) The programmable current sink is the input characteristic of a "lossless energy converter" (detailed in Figure 2b). The energy converter intercepts instantaneous power from the power line, which is the product of the instantaneous voltage and the instantaneous current entering the energy converter. All energy intercepted by the energy converter is delivered to the load device.

Although the devices detailed in Figures 2a and 2b emulate resistors, they provide no means of controlling the overall level of power intercepted from the power line. The circuit in Figure 2c allows for variation in both line voltage and load power. The "load device" detailed in Figures 2b and 2c is invariably a low AC impedance device; such devices include, but are not limited to, capacitors, batteries, and voltage sources.

The overall goal of PFC is to transfer power from a "wiggly" source such as an AC power line to a relatively benign DC voltage. This task must be performed without stuffing a bunch of harmonic junk back on the AC power line.

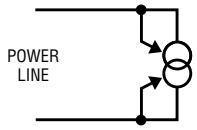


Figure 2a. Programmable current sink

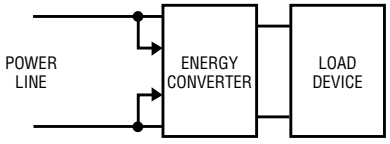


Figure 2b. Non-programmable energy converter (aka PFC)

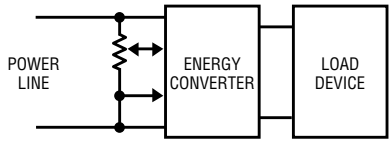


Figure 2c. Programmable energy converter (aka PFC)

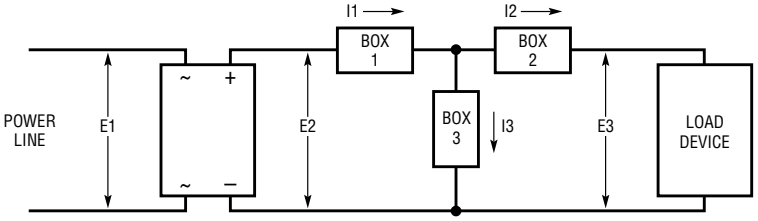


Figure 3. Detailed block diagram of energy converter

The Energy Converter Box

How it Works

The energy converter shown in Figure 2b obeys the laws of conservation of energy (as we all must). As the energy intercepted at the input is transformed from one voltage to another, the current is also transformed from one value to another. The energy stays the same.

The "guts" inside the energy converter block of Figure 2b are further detailed in Figure 3. Regardless of the circuitry in boxes 1–3, we can be sure that Kirkhoff will have his way: I1 + I2 + I3 = 0. Further, we shall assume that whatever occupies the three boxes is lossless (a pretty good assumption in a PFC with better than 95% efficiency). Since the energy intercepted from the input power line E1 cannot be dissipated in the lossless contents of Boxes 1, 2, and 3, it will be losslessly transferred to the output E3.

Figure 4 illustrates the waveforms of a 300W, 120V-to-382VDC power conditioner (refer also to Figure 3). Figure 4a shows E1, the input power line voltage of $120V_{RMS}$. Figure 4b details E2, the full-wave-rectified sine wave.

The energy converter does magic things in the three boxes to cause the waveshape of the input current I1 (Figure 4c) to be a replica of the input voltage E2, with only the magnitude being different. The power intercepted from the input is P1:

P1 = I1 × E2 (see Figure 4d).

Note that the input power is a sinusoidal waveshape, is always positive, and is at twice the line voltage frequency. This is exactly what the waveshape and frequency of the power delivered from a sine wave source to a resistive load looks like.

All of the power intercepted by the energy converter circuit is transferred

continued on page 21

PFC: (Power Factor Correction)— The process used to make capacitors look like resistors. PFC became popular in the early 1990's when the earthlings realized that about 10% of the power they harnessed on their planet was being converted to heat. This heat, which was dissipated through their power distribution network, become a contributing factor in their global warming trend. (see *History of the Sol System*, Vol. 17, pp. 137,657–137,698.)

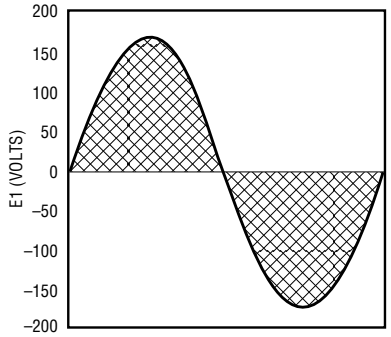


Figure 4a. E1, input voltage waveform: 300W idealized PFC

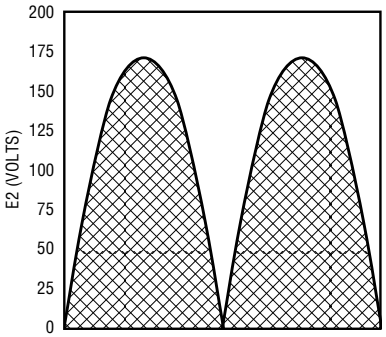


Figure 4b. E2, full-wave-rectified sinewave: 300W idealized PFC

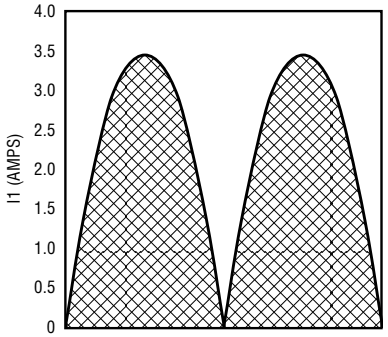


Figure 4c. I1, input current: 300W idealized PFC

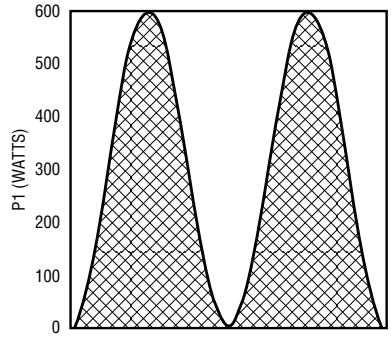


Figure 4d. P1, power intercepted from the input (P1 = I1 × E2): 300W idealized PFC

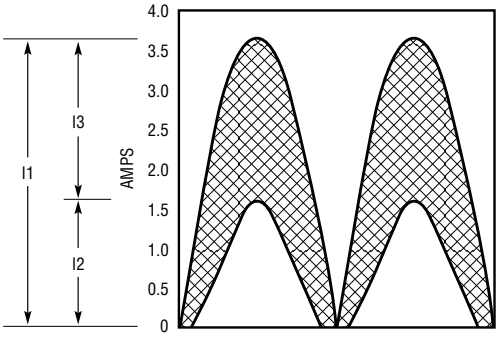


Figure 4e. Input current, I1, and output current, I2. I3 is obtained by subtraction. 300W idealized PFC

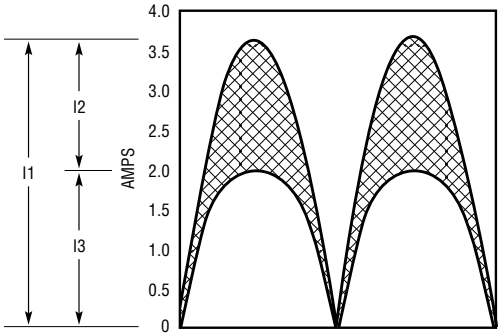


Figure 4f. Input current, I1, and current through Box 3, I3. I2 is obtained by subtraction. 300W idealized PFC

Power for Pentium™

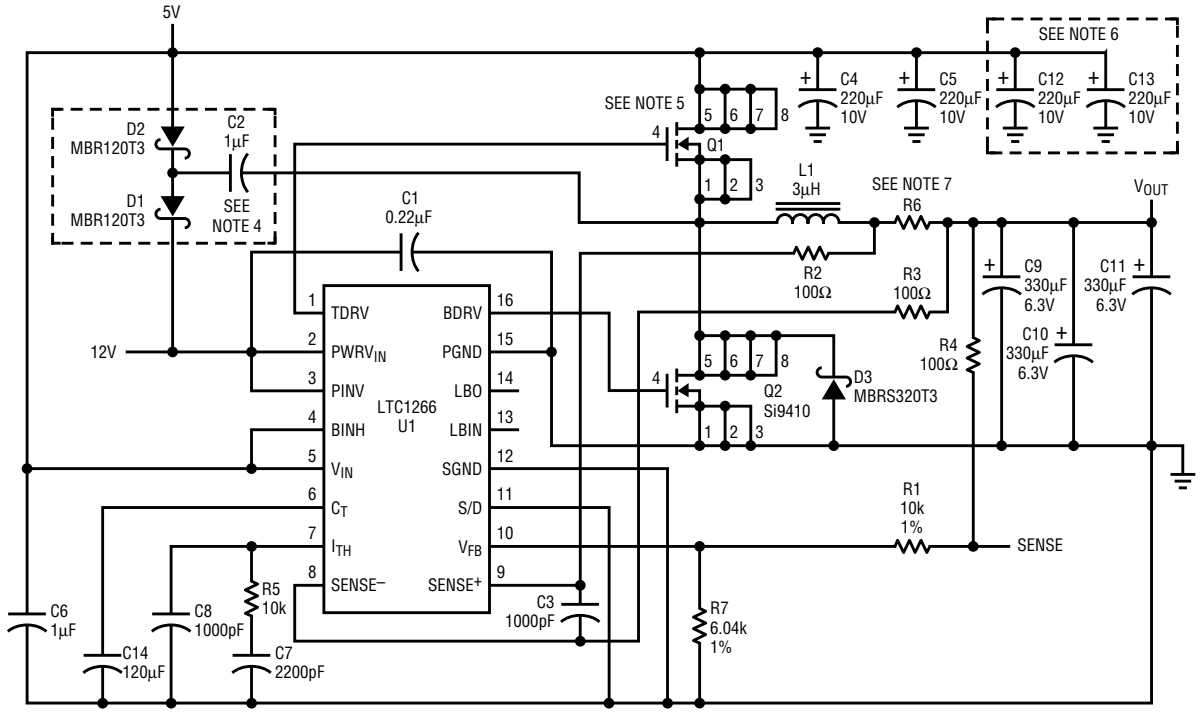
by Craig Varga

Introduction

Providing power for the Pentium microprocessor family is not a trivial task by any means. In an effort to simplify this task we have developed a new control circuit and spent considerable time developing an optimized decoupling network. Here are several circuits using the new LTC1266 synchronous buck-regulator control chip to provide power for the P54C, P54C-VR, and P54C-VRE microprocessors. The P54C has a supply requirement of 3.3V ±5%, the P54C-VR requires 3.3V +5%/–0%, and the P54C-VRE requires 3.525V ±75mV.

LTC1266 Drives N-Channel MOSFETs

The LTC1266 controller offers several advantages over its predecessors. First, it will drive all N-channel MOSFETs instead of requiring P-FETs for the high side switches. This lowers cost and improves efficiency. It also has an improved, higher-gain error amplifier, which results in better load regulation, compared to that of the LTC1148 family. There is also an undedicated comparator, which may be used for a "power-good" monitor or an overvoltage detector in these applications. There is a shutdown pin and a new burst-inhibit function. Burst mode is inhibited on all the designs shown here, but for the P54C supplies, (non-VR/VRE parts) burst may be enabled if desired, resulting in improved light-load efficiency. This is done by tying pin 4 low. The reference tolerance available on the LTC1266 (or on any other PWM controller, for that matter) is not accurate enough for the -VR or -VRE specifications. The LT1431, however, has a sufficiently accurate reference for these applications, and permits very effective remote sensing (see Figure 2). Do not enable Burst Mode on the



NOTES:
1. CIRCUIT SHOWN IS 5V TO 3.3V AT 5A OR 10A, ±5%.
2. ASSUMES APROX. 400 µF OF TANTALUM CAPACITOR IN µP SOCKET CAVITY IN ADDITION TO OUTPUT CAPACITORS SHOWN ON POWER SUPPLY.
3. ALL POLARIZED CAPACITORS ARE AVX TYPE TPS OR EQUIVALENT.
4. IF 12V IS AVAILABLE, THESE PARTS MAY BE ELIMINATED.
5. FOR 5A OUTPUT USE Si9410. FOR 10A, USE Si4410.
6. PARTS MAY BE ELIMINATED IN 5A DESIGN.
7. VALUE FOR 5A IS 0.02 Ω. FOR 10A USE 0.01Ω.

Figure 1. Pentium P54C 5/10 amp power supply circuit

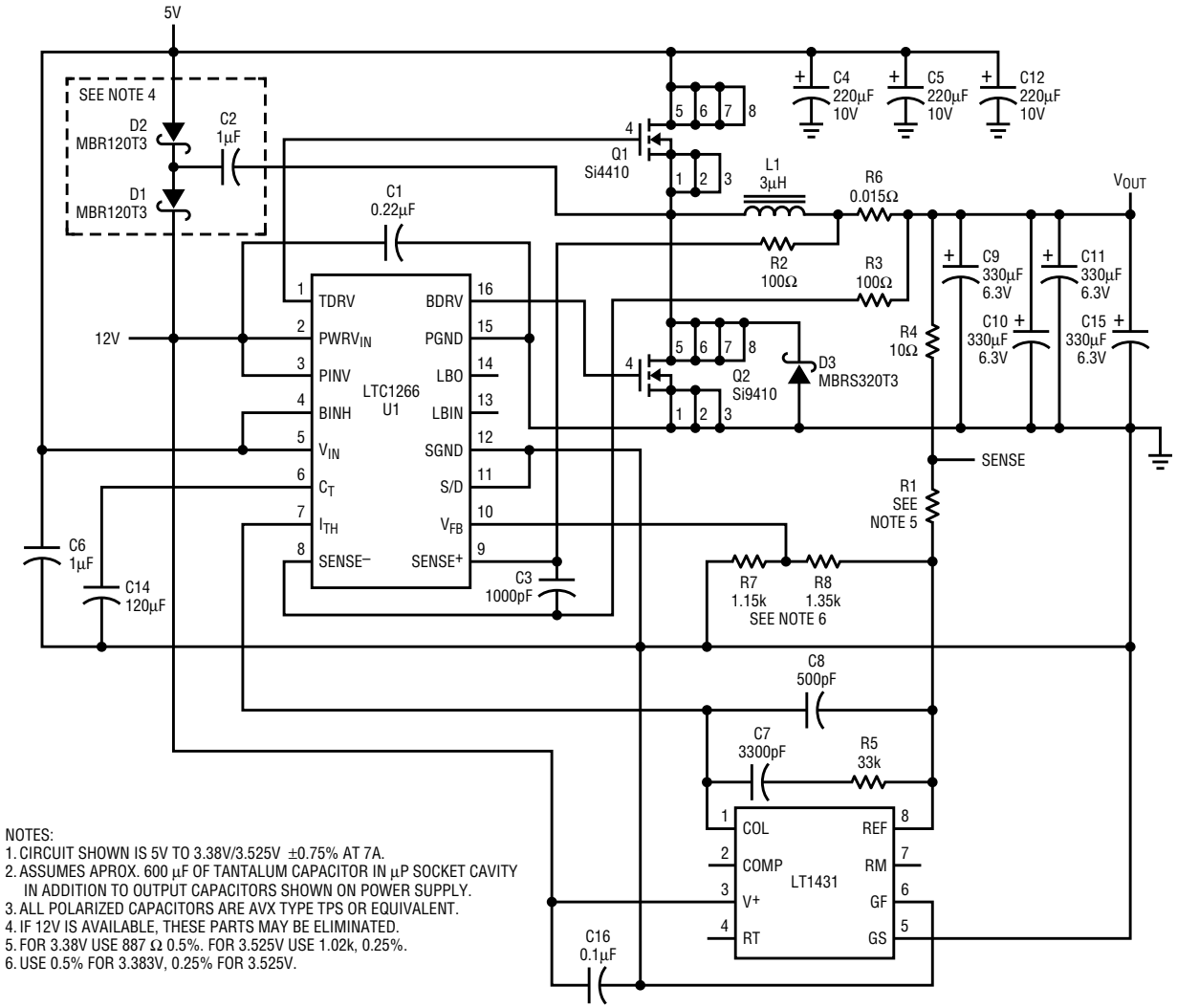


Figure 2. Pentium P54C-VR and P54C-VRE 7 amp power supply circuit

circuits designed for the P54C-VR or -VRE using the LT1431-based supplies, as the designs shown will not operate correctly at no load.

Handling the Load Transients

The Pentium processor has several nasty habits that require careful attention if the circuit is to be reliable. The main problem is the load transients that the processor generates. It can go from a low power (200mA) state to nearly 4 Amps in two clock cycles or 20 nanoseconds. While all this is going on, the supply voltage must be held within the spec limits. For the P54C-VR spec, the set point is 3.38V with a 2.5% tolerance. The -VRE spec is even tighter. These specs include line, load, and temperature regulation and initial set-point tolerances, as well as transient response. As may be imagined, meeting this requirement is not a trivial task. With only 2% total deviation from the ideal voltage allowed, the static specifications (line, load, temperature, and initial set-point) must be held to approximately ±1% if any amount of transient response is to be permitted.

Realistically, approximately 40mV peak transient response is obtainable. To achieve this, a large number of low-ESR tantalum capacitors must be installed as close to the processor as possible. The microprocessor socket cavity is the best place. As an absolute minimum, use six 100µF, 10V AVX type TPS tantalums. If more height is available, as with a ZIF socket, it is preferable to use six 220µF, 10V parts instead. With the 100µF parts there is very little margin in the design. Do not reduce the quantity of the capacitors if going to a larger value. The ESR specs are the same for the 100µF, 220µF, and 330µF capacitors. The reason for paralleling six caps is to reduce the ESR as well as to provide bulk capacitance. In the case of standard P54C applications, a slightly larger transient can be tolerated, so somewhat less capacitance can be used. We recommend that you use at least four 100µF AVX tantalums. In all cases there should be ten 1µF ceramic capacitors to decouple the high-frequency components of the transient.

Circuit-Board Layout Considerations

All the capacitors in the decoupling network should be installed on power- and ground-plane areas on the top side of the board. An absolute minimum of one feedthrough per end for each capacitor into the internal power and ground plane should be used. It is preferable to use two feedthroughs per capacitor end (64 total). Any more than that proves to be of no benefit, but at 30 total, expect about a 2mV increase in transient droop. This is about a 5% degradation in performance. Decoupling capacitors should be connected with planes rather than traces, since the traces will be far too inductive. The total network ESR must be less than 6.5 milliohms and the total ESL less than 0.07 nanohenry for the P54C-VR.

Input Capacitance

Another important consideration is the amount of capacitance on the power supply input. The ripple-current rating must be high enough to handle the regulator input ripple. In addition, this capacitance will decouple the load transients from the 5V supply. If insufficient capacitance is used, the disturbance on the 5V supply will exceed the 5% specification for the TTL logic powered by this voltage. Because the magnitude of this disturbance is quite dependent upon the nature of the 5V power supply and because the performance of these supplies varies widely, it is difficult to say just how much capacitance is needed. In general, however, if enough capacitance is present to handle the ripple current, the disturbance on the 5V supply will be acceptable. Good transient response on the 5V supply translates to a need for less input capacitance. If sufficient bulk capacitance is present on the motherboard for the 5V supply, less additional capacitance will be required on the processor supply input. As a minimum, there should be at least one low-ESR capacitor within an inch of the regulator. Be careful to look at the level of disturbance on the 5V supply to make sure it remains within specifications.

Powering the P54C

The same basic circuit is used for both the 5 Amp and the 10 Amp designs. The necessary substitutions are shown on the schematic (Figure 1). If 12V is available to power the LTC1266, the bootstrap capacitors and diodes can be eliminated. The 12V solution is preferred, as it is simpler and somewhat more efficient. If no 12V is available, use the bootstrap circuit. Note also that different MOSFETs are specified for the 5 Amp and 10 Amp circuits. The Si4410 is a new part from Siliconix, which offers less than half the on-resistance of the Si9410 used in the 5 Amp circuit.

High-Accuracy Solution—Basics of Operation

The solution for the P54C-VR and -VRE shown in Figure 2 relies on the accuracy of the LT1431. The internal reference is specified at 2.5V ±0.4% (worst case) at 25°C. The LT1431 consists of a precision reference and a wide-bandwidth amplifier with an open-collector output. The feedback divider is set to place the reference input pin at 2.5V with the desired output present. The 2.5V is further divided to 1.15V to drive the LTC1266s VFB pin. In a normal application, this pin will servo to 1.25V. Hence, the LTC1266 sees the output as being too low and forces its internal error amplifier to the positive rail, which, in this case, is 2.0V. This output shows up as a current out of the I_{TH} pin. The open collector of the LT1431 draws enough current from this pin to set the output of the supply at the desired voltage. Since this constitutes a high-gain servo loop, the output is regulated very accurately. Loop compensation is accomplished by R5, C7, and C8. The internal error amplifier of the LTC1266 will act as an overvoltage protection loop should the LT1431 ever fail.

Conclusion

The Pentium microprocessor offers some interesting challenges to the power system designer. To operate the microprocessor at higher clock speeds requires very stringent supply voltage specifications. Stop-clock power saving modes have introduced severe load transients not present in older generations of processors. However, with careful attention to detail both in component selection and mechanical layout, the required performance can be obtained. Also, the need for high efficiency can be met while providing the required dynamic performance. LT

PFC, continued from page 18

to the output. Therefore, the input power, P1, flows into the load device, E3, as output current I2. Further, since E3 is a constant voltage, I2 will have a waveshape that is identical to P1. Figure 4e details the input current I1 and the output current I2. By subtracting I2 from I1 we can see what I3 looks like. Figure 4f details the input current I1 and the current through box 3 (I3).

This is the first in a series of articles explaining power-factor correction. The next article will present more component level circuitry using the LT1248 and LT1249 PFC devices. In the meantime, if you require more information contact the LTC factory. LT

PCMCIA Socket Voltage Switching Matrix with SafeSlot™ Protection

by Doug La Porte

Introduction

Most portable computer systems have built-in PCMCIA sockets as the sole means of expansion. The designers of these portable systems are demanding more integrated solutions for PCMCIA-socket voltage switching. In addition, many experienced designers are requiring some means of protecting their systems from meltdown when users connect damaged cards.

Host power delivery to the PC card socket flows through two paths: the main V_{CC} supply pins and the VPP programming pins. Both supplies are switchable to different voltages to accommodate a wide range of card types. The V_{CC} supply is the main supply and must be capable of providing up to 1A at either 3.3V or 5V, as well as realizing a high impedance state. The 1A rating is an absolute maximum derived from the contact rating of 500mA per pin for both V_{CC} pins. One of the most stringent actual requirements is hard-disk drive spin-up current. Present hard drives require 5V at 600–800mA for a short duration during spin-up. Current draw drops to 300–420mA during read and write operations. The VPP supply must source 12V at up to 120mA, 3.3V, or 5V at lesser currents, 0V, and realize a high-impedance state. The VPP supply is intended solely for flash-memory programming. The 120mA current requirement allows erasing two flash devices and writing to two devices simultaneously, as required by many flash drives.

The host PCMCIA socket designer must also consider several other practical aspects of the design. The socket pins are exposed to the outside world and users may have little or no technical knowledge. The socket pins are vulnerable to being shorted by foreign objects, such as paper clips. In addition, users may attempt to install damaged, possibly short-circuited, cards. In short, once the product is in the hands of the consumer, the designer and manufacturer have little control over use and abuse. To ensure a robust system and a satisfied customer, PCMCIA switch protection features such as current limiting and thermal shutdown are a necessity. These features will protect the card, socket, and main system power supply.

The nature of PC cards and portable systems requires the card to be powered on and off, as needed, to con-serve power. With many PC cards drawing over 2W, this power up/down sequencing can put demanding transient requirements on the system power supply. To make the transient response of the system supply manageable, the PCMCIA switch should have break-before-make switching with controlled rise and fall times. Controlled rise and fall times eliminate the possibility of the main supply being momentarily pulled down by a switch transient, triggering a system reset.

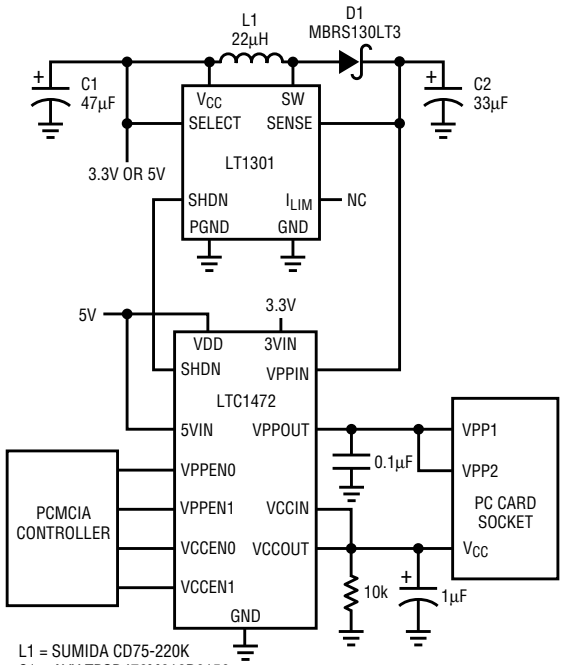


Figure 1. Typical LTC1472 application with the LT1301 3.3V/5V boost regulator

LTC1472: Complete V_{CC} and VPP PCMCIA Switch Matrix with SafeSlot Protection

The LTC1472 is a complete V_{CC} and VPP switch matrix that addresses all PCMCIA socket switching needs. The part is fully integrated, with no need for external switching FETs. The V_{CC} switch's $R_{DS(ON)}$ is 140mΩ to support the current requirement of up to 1A. The V_{CC} output is switched between 3.3V, 5V and high impedance. The VPP 12V switch's $R_{DS(ON)}$ is 0.5Ω to support its current requirement. The VPP output pin is switched among 0V, V_{CC}, 12V, and high impedance. Table 1 shows the V_{CC} and VPP truth tables. The V_{CC} logic inputs are exclusive-ORed to allow direct interfacing with both logic-high and logic-low industry standard controllers without any external glue logic. The LTC1472 is available in the space-saving narrow 16-pin SOIC package.

The LTC1472 features SafeSlot protection. The built-in SafeSlot current-limiting and thermal-shutdown features are vital to ensuring a robust and reliable system. The V_{CC} current limit is above the 1A socket limit to maintain compatibility with all existing cards yet provide protection. For the same reason, the VPP current limit is above 120mA. All switches are break-before-make types with controlled rise and fall times for minimal system supply impact.

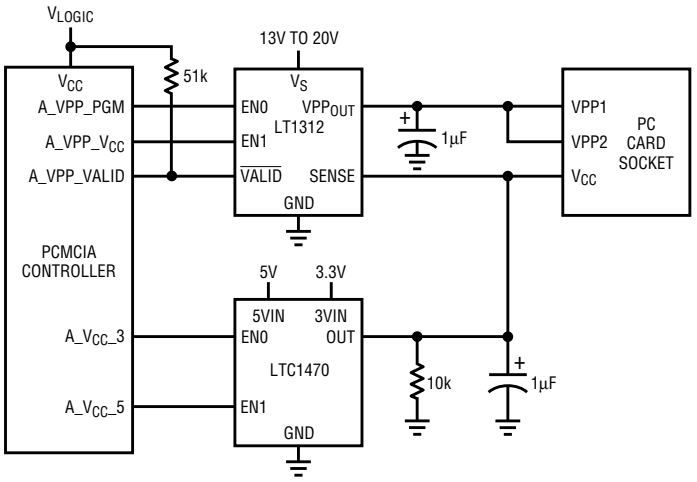


Figure 2. Typical LTC1470 application with the LT1312 VPP driver/ regulator

Figure 1 shows a typical LTC1472 application used in conjunction with the LT1301 to supply the 12V input. The LT1301 is optional. If the system already has a suitable 12V supply, it can be directly connected to the VPP_{IN} pin. Be cautious when using a general purpose 12V supply; make certain that it does not have spikes or transients exceeding the flash-memory 14V maximum voltage rating and that the regulation is within the 5% flash memory tolerance.

The LTC1472 does not require a continuous 12V supply. The device has on-chip charge pumps running from the 5V supply for driving the switches. For this reason the LT1301 is usually in shutdown mode, consuming only 10µA. The LT1301 becomes operational only when the controller programs the LTC1472 to deliver 12V to the VPP pin. The LTC1472 also conserves power by going to a low 1µA standby mode when both V_{CC} and VPP outputs are switched off. The schematic in Figure 1 includes a 10kΩ pull-down resistor on the $V_{CC\ OUT}$ pin. This resistor will ensure that, when switching the V_{CC} voltage from 5V to 3V, the voltage will not float at 5V. The current PCMCIA specification requires the voltage to be pulled down to 0.8V within 300ms. The pull-down resistor is adequate to ensure proper operation.

LTC1470: V_{CC} Switch Matrix with SafeSlot Protection

For systems where VPP switching is not required, the LTC1470 is the optimal solution. The LTC1470 is a complete V_{CC} switch matrix. It is fully integrated, with no need for external switching FETs. Performance specifications are the same as those of the V_{CC} section of the LTC1472 described above. The switch has an $R_{DS(ON)}$ of 140mΩ to support the V_{CC} current requirements of up to 1A. Table 2 shows the truth tables for both logic-low- and logic-high-type controllers. The LTC1470 is available in the space-saving 8-pin SOIC package.

Like the LTC1472, the LTC1470 also features SafeSlot protection. The switches are break-before-make types with controlled rise and fall times for minimal system power supply impact. The built-in SafeSlot current-limiting and thermal-shutdown features are vital for a robust and reliable system.

Figure 2 shows a typical LTC1470 application with the LT1312 used to control the VPP section. The LT1312 is a linear regulator designed specifically for PCMCIA VPP voltage switching. This device requires an input voltage greater than 13V. If your application does not require VPP switching, the LT1312 can be eliminated. The LTC1470 has on-chip charge pumps for driving the switches. Only the 3.3V and the 5V inputs are required. The LTC1470 conserves power by going to a low 1µA standby mode when the output is switched off. The schematic in Figure 2 includes a 10kΩ pull-down resistor on the $V_{CC\ OUT}$ pin to guarantee that the V_{CC} voltage will not float when turned off.

Conclusion

PCMCIA sockets are becoming more common as the preferred method of expansion in portable systems. As these devices proliferate to less sophisticated users, there will be greater opportunities for abuse. To counter this trend, the portable system designer must take precautions to protect the system. The high level of integration, SafeSlot protection features, and controlled rise and fall time switching make the LTC1470 and LTC1472 ideal solutions for portable systems.

Table 1. LTC1472 truth table

V_{CC} Switch Truth Table			VPP Switch Truth Table		
VCCEN0	VCCEN1	VCCOUT	VPPEN0	VPPEN1	VPPOUT
0	0	OFF	0	0	0V
1	0	5V	0	1	VCCIN
0	1	3.3V	1	0	VPP_{IN}
1	1	OFF	1	1	HiZ

Table 2. LTC1470 truth table

CL-PD6720 Controller			"365-Type" Controller		
$A\_V_{CC}\_3$ (EN0)	$A\_V_{CC}\_5$ (EN1)	OUT	$A\_V_{CC}\_EN0$ (EN0)	$A\_V_{CC}\_EN1$ (EN1)	OUT
0	0	HiZ	0	0	HiZ
1	0	5V	1	0	5V
0	1	3.3V	0	1	3.3V
1	1	HiZ	1	1	HiZ

LTC's RS232 Transceivers for DTE–DCE Switching

by Gary Maulding

Introduction

EIA/TIA-232-E (commonly known as RS232) is the most commonly used serial data-communications standard. The standard defines signal levels and connectivity between a data terminal (DTE) and a piece of communications equipment (DCE). A cable of up to 25 lines connects the DTE and DCE. Each wire's function (data, control, or ground), pin assignment, and direction of signal flow are defined by the standard, but the software protocol used to transfer information is left unspecified.

System Configuration

Few systems use all of the signaling lines available. The most common configuration uses nine wires, eight for signals plus one for ground. This configuration is compatible with the 9-pin serial ports on IBM PC/AT-compatible computers. Two wires are used for data transmission (one in each direction), two wires transfer control information from DTE to DCE, and four wires transfer control information from DCE to DTE. Figure 1 defines the pin assignments between a 9-pin AT connector at the DTE and a 25-pin connector at the DCE.

The EIA-232-E standard does not define whether a piece of equipment is a DTE or a DCE. In a conventional computer-to-modem link the roles are clear: the computer is the DTE, and the modem the DCE. This might lead one to think that a computer would always be a DTE, but this is not true. An RS232 serial link can be used to communicate between two computers. In this case, one computer must be a DTE, and other a DCE. A Printer is usually configured as a DTE, forcing the computer to appear as a DCE device. This dual nature of an AT serial port is possible because few systems use all of the data and control lines available. In order to facilitate the various connections between equipment, special cables are used to connect various devices in the proper ways. For example, a null modem cable enables two PCs to communicate by cross wiring several lines (see Figure 2), contracting the number of independent signal lines to six, (three in each direction). The Ring Indicator and Carrier Detect signals are lost.

Only Linear Technology's RS232 transceiver circuits make switching between a DTE and a DCE port this easy

Switched DTE/DCE Port

There are situations where a data port is required to act alternately as either a DTE or a DCE. Examples include test equipment and data multiplexers. Figure 3 shows a circuit that can switch from a 9-pin DTE to a 9-pin DCE configuration while maintaining full compliance with the RS232 standards.

The circuit uses an LT1137A DTE transceiver and an LT1138A DCE transceiver. A DTE/DCE select-logic signal alternately activates or shuts down one of the two transceivers. In addition to drawing no power, the OFF transceiver's drivers achieve a high impedance state, removing themselves from the data line. The receiver inputs will continue to load the line, but this presents no operational problem and does not violate the RS232 standard. The drivers on the activated transceiver can easily drive the extra load of the companion transceiver's inputs along with the termination at the opposite end of the cable. The scope photograph [Figure 3b) shows the signal outputs of the DTE-DCE switched circuit driving 3kΩ||1000pF at 120kbaud.

To the transceiver at the opposite end of the data line, the data port always appears to be a normal fixed port. All signals into the port are properly terminated in 5k.

The schematic in Figure 3a shows the essential features needed to implement DTE-DCE switching, but other features can be easily included. Shutdown of both transceivers could be implemented by adding an additional logic-control signal. Multiplexing of the logic-level signals is also possible, since receiver outputs remain in a high impedance state when the transceivers are shut down. Two capacitors can be saved by sharing the V+ and V– filter capacitors between

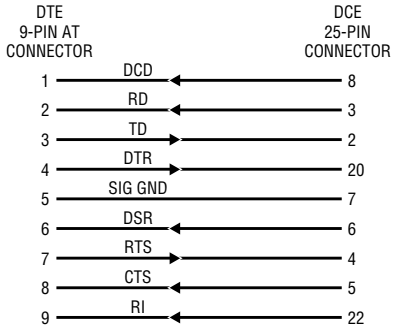


Figure 1. RS232 pin assignments: DTE 9-pin connector and DCE 25 pin connector

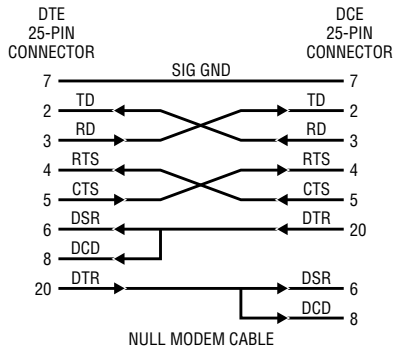


Figure 2. Null modem cable allows two PCs to communicate

Conclusion

the two transceivers, but the charge-pump capacitors must not be shared.

The circuits used in the demonstration circuit are bipolar, but Linear Technology's CMOS transceivers, such as the LTC1327 and 1328 could be substituted where the absolute minimum power dissipation is required.

Only Linear Technology's RS232 transceiver circuits make switching between a DTE and a DCE port this easy. All of Linear Technology's transceivers include drivers that achieve a high-impedance state when shut down. The design differences between LTC's drivers and the competition's are shown in Figure 4. The conventional drivers' CMOS body diodes do not allow the outputs to go high impedance when off. The manufacturers of these transceivers guarantee only a 300Ω impedance when off, prohibiting the multiplexing of drivers on one line.

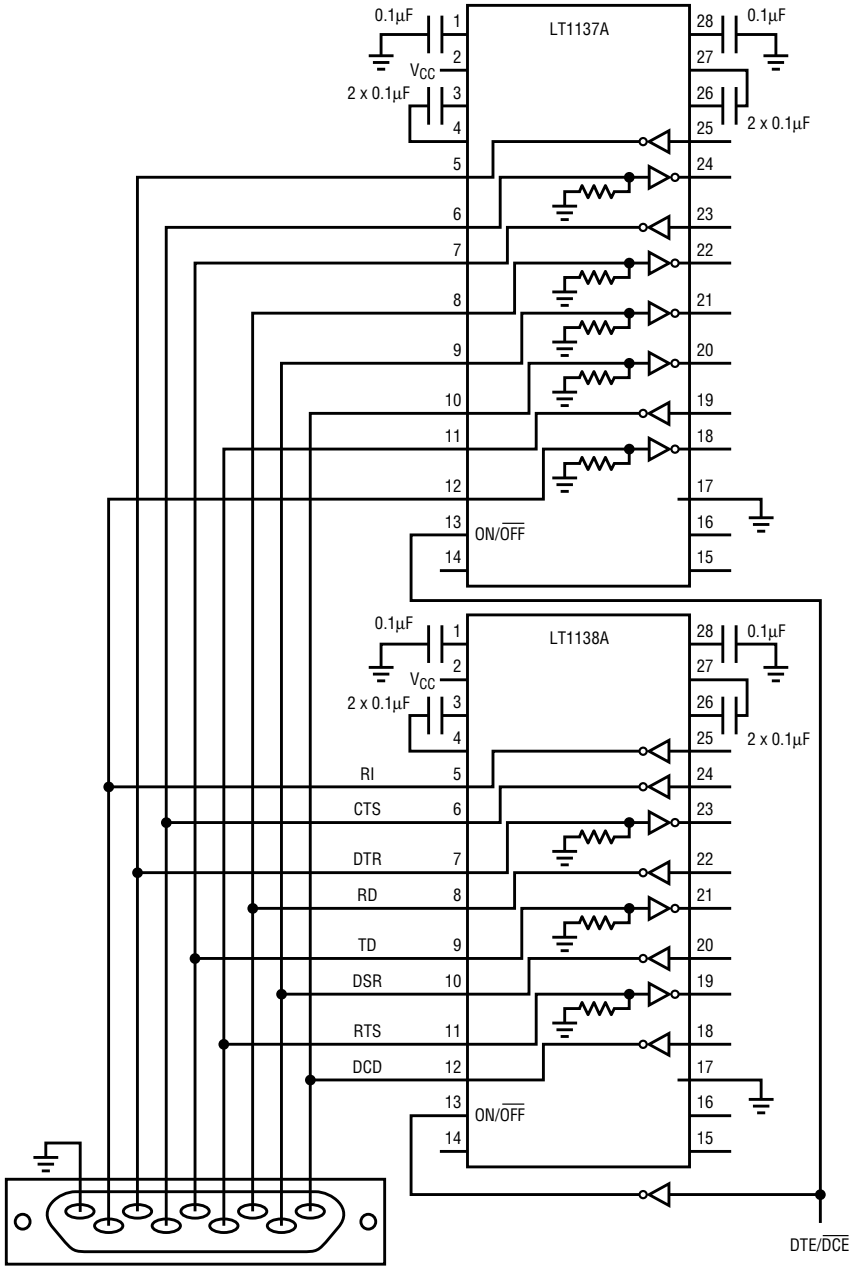


Figure 3a. Switchable, 9-pin DTE/DCE data-port circuitry

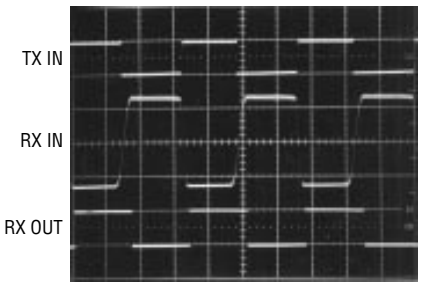


Figure 3b. Oscillograph showing signal outputs of the DTE-DCE circuit of Figure 3a driving 3K || 1000pF at 120kbaud

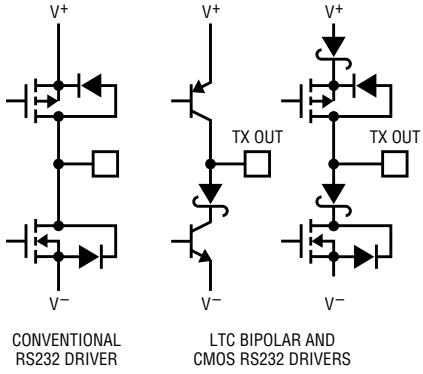


Figure 4. Conventional versus LTC bipolar and CMOS RS232 drivers

LTC Provides Two Crucial Components for HDSL Systems

by Kevin R. Hoskins

HDSL Description

High bit-rate Digital Subscriber Line (HDSL), an extension of ISDN, allows high data-rate digital transmission over ordinary, ubiquitous, twisted-copper-pair telephone lines. HDSL is designed to interconnect a central office and nearby sites or to connect customers to a remote digital terminal. Although HDSL's transmission speed cannot match that of fiber optics, the use of existing copper pairs delays the costs of upgrading to fiber optics.

Although HDSL uses the same ISDN digital-subscriber line (DSL) and 2-bits-and-1-quaternary (2B1Q) coding to transmit DS1 signals, it does so at 1.544Mb/s (two 784Kb/s dual duplexes) instead of ISDN's 160Kb/s. Further, the twisted-copper pairs over which HDSL signals are transmitted do not require preconditioning and can reach lengths of 12,000 feet (24-gauge wire) or 9,000 feet (26-gauge wire). An echo canceller and hybrid located in the interface circuit between the phone lines and a network interface help ensure that the HDSL circuitry accomplishes full duplex transmission.

HDSL is more tolerant of error-causing perturbations and is easier to implement than standard T1 data transmission methods. HDSL installation is also very easy and labor efficient. As long as the digital loop carrier (DLC) system into which the HDSL is installed follows carrier service area (CSA) guidelines, HDSL does not require field servicing and installation is much faster. Additionally, HDSL can use copper pairs whose lengths are unequal, unlike a T1 system

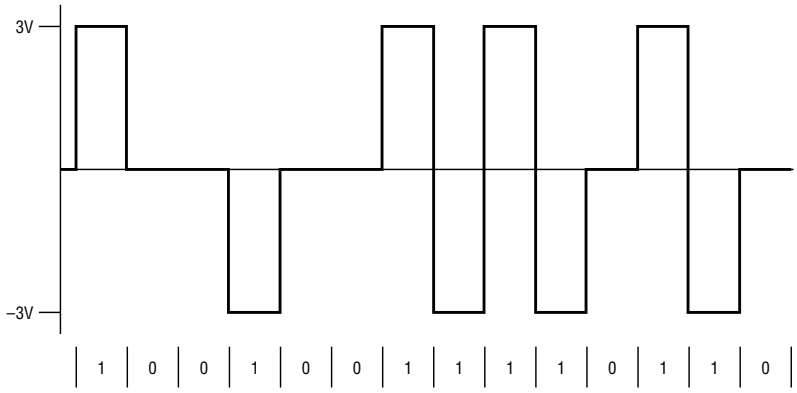


Figure 1. Alternate mark Inversion (AMI) or bipolar encoded transmissions

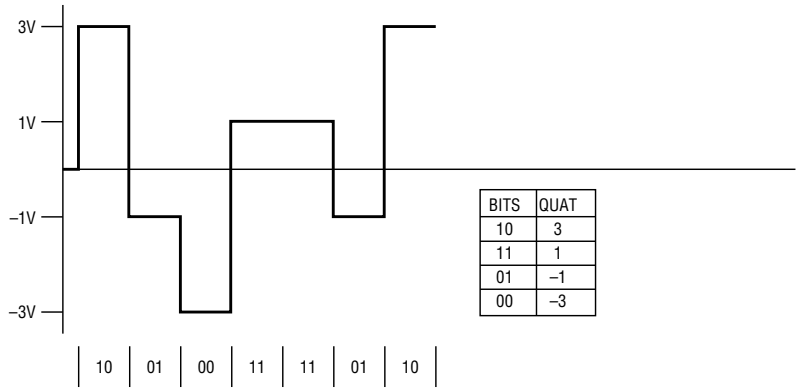


Figure 2. HDSL's more efficient 2B1Q encoding

HDSL Coding Doubles Data Rate

HDSL's coding scheme is more efficient than some other schemes, such as alternate mark inversion (AMI—also known as bipolar), used by DS1 transmissions. AMI's encoding is bit-for-bit, as shown in Figure 1. This results in a transmission frequency that is one-half the transmitted bit rate. For example, a 160Kbit/s transmission rate equals an 80kHz transmission frequency.

In contrast, HDSL uses a 2B1Q transmission-coding scheme. This scheme further reduces the transmission frequency, allowing more data conveyance over the same bandwidth. Figure 2 shows the HDSL coding scheme. Using one-half the number of bits of an AMI signal, HDSL transmission frequency is one-half the AMI transmission frequency. Therefore, to extend our previous example, the 80kHz transmission frequency of AMI becomes 40kHz for HDSL.

Whereas the data recovery relies heavily on digital signal processing (DSP), the HDSL receiver and transmitter circuitry preserve the integrity of the data supplied to, and by, the DSP. The receiver's analog front-end circuitry assumes this guardian role. This circuitry consists of lowpass filters, transformer drivers, and analog-to-digital converters.

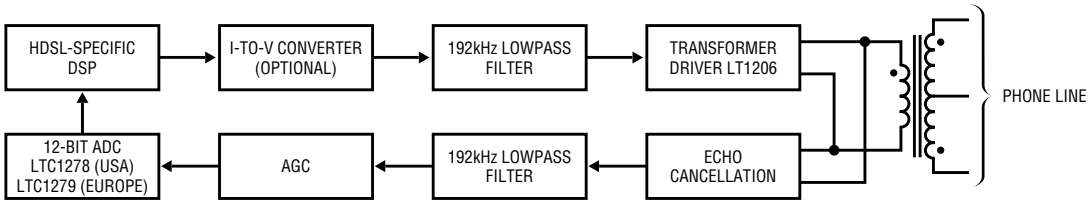


Figure 3. HDSL block diagram

Two Crucial Components for Your Solution

Figure 3 shows a block diagram of a typical HDSL receiver/transmitter. Central to the design is the analog signal processing circuitry that conditions and converts the received transmissions into digital data understood by the HDSL-specific DSP. The major components of the system include transmit and receive lowpass filters, automatic gain control (AGC), a 12-bit ADC, and a DSP.

The received path begins by transformer-coupling the received signal to an echo canceller. The echo canceller uses phase delay and differential amplification to reduce error-inducing transmission echoes. The echo canceller's output is applied to a lowpass filter. The 12-bit ADC digitizes the filter's output and applies it to the DSP. The DSP recovers the quaternary information from the digitized signal and converts it to the original bit pattern. The AGC block compensates for variable line attenuation. This can be implemented in various ways: the filter can be configured to perform AGC, a separate adjustable-gain stage can be inserted between the filter output and the ADC, or the ADC's reference voltage can be adjusted.

HDSL is more tolerant of error-causing perturbations and is easier to implement than standard T1 data transmission methods... installation is very easy and labor efficient

The transmit path begins with a DSP-generated output signal (either a current or voltage) applied to a lowpass filter similar to that found in the receive path. The output of the filter is then applied to an amplifier that drives the coupling transformer's impedance.

Driving the Line with Low Distortion

Linear Technology has the ideal component for driving the line-coupling transformer. The LT1206 is a 40MHz current feedback op amp with a 250mA, source-and-sink output-drive capability. With this output-drive capability, the LT1206 can easily drive the transformer's 135Ω impedance, typical for transformers designed for HDSL applications. The LT1206 is available in a space-efficient, SO-8 surface-mount package.

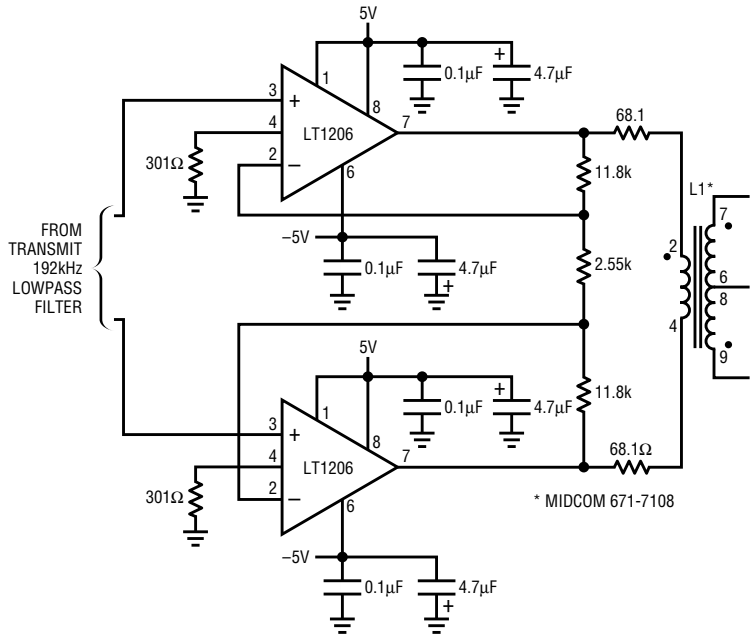


Figure 4a. LT1206 used as a differential HDSL transformer driver

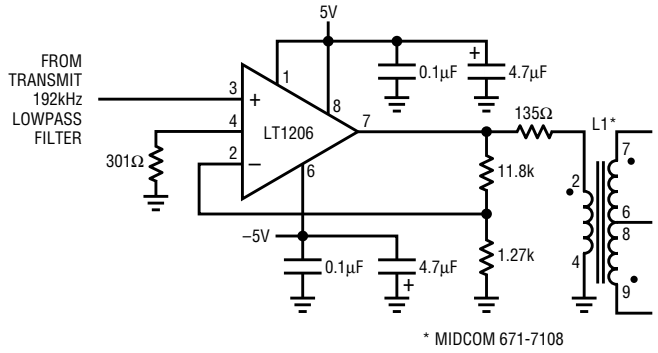


Figure 4b. LT1206 used as a single-ended HDSL transformer driver

The HDSL analog signal path between the DSP output and the transformer input can be differential or single-ended. Figure 4 shows the LT1206 driving an output transformer in differential and single-ended modes. Because of even-order-distortion cancellation, the differential operation can achieve better performance than that of the single-ended operation. However, the LT1206's output-drive capability is so robust that singled-ended operation is very effective, reducing cost, board space, and power dissipation.

Digitizing the Received Signal with Very Low Errors

The 12-bit LTC1278's 400ksps sampling rate can easily handle the 1.544Mb/s bit rate (392ksps symbol rate) used in the USA (T1), whereas the 12-bit LTC1279's 600ksps takes care of Europe's 2.048 Mb/s bit rate (584Kb/s base bit rate).

Should HDSL's transmission speed increase in the future, LTC will have an ADC solution. Elsewhere in this issue is an article discussing the features and speed of the LTC1410. This 12-bit ADC has a minimum conversion rate of 1.25MHz, a parallel interface similar to that of the LTC1278 and the LTC1279, and dissipates only 150mW (typical). (See this issue's lead article for complete information.)

Provisions for AGC are present in some of the HDSL-specific DSPs. Typically, the control consists of two digital outputs whose output-logic levels change according to the received HDSL signal's magnitude. These logic signals can be used to easily implement 6dB of AGC by adjusting the ADC's reference voltage. A 6dB gain increase corresponds to a reference voltage change of one-half.

Figure 4 shows a 2N3906 PNP transistor configured to alter the LTC1278's reference voltage and accomplish a 6dB change in the ADC's output code. For 0dB gain, a logic low is applied to the transistor's base, turning it on. The +5V power supply voltage, minus the transistor's saturation voltage, is applied to the LTC1278's reference output pin, overriding the internal reference. Full-scale positive and negative digital output codes occur at ±4.8V input signal levels. When the DSP determines that 6dB of gain is necessary, it applies a logic high to the transistor's base, turning it off. The LTC1278 now uses its internal reference in the conversion process. Full-scale positive and negative digital output codes occur at ±2.5V input signal levels.

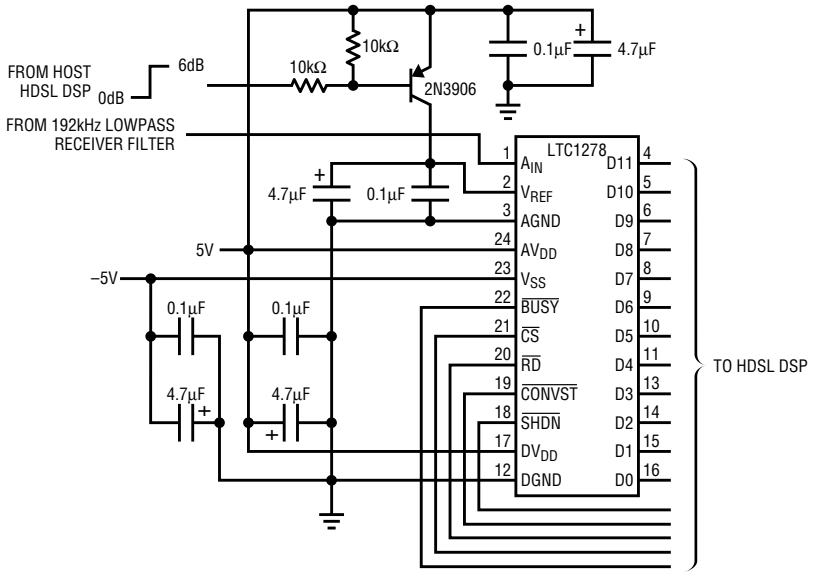


Figure 5. LTC1278 circuit with programmable gain

Sensing Negative Outputs

by Dimitry Goder

Various switching regulator circuits exist to provide positive-to-negative conversion. Unfortunately, existing controllers usually cannot sense the negative output directly; the majority of them require a positive feedback signal derived from the negative output. This creates a problem. The circuit presented in Figure 1 provides an easy solution.

The LT1172 is a versatile switching regulator, which contains an onboard 100kHz PWM controller and a power switching transistor. Figure 1 shows the LTC1172 configured to provide a negative output using a popular charge-pump technique. When the switch turns on, current builds up in the inductor. At the same time, the charge on C3 is transferred to output capacitor C4. During the switch off-time, energy stored in the inductor charges capacitor C3. A special DC level-shifting feedback circuit consisting of Q1, Q2, and R1–R4 senses negative output voltages.

Under normal conditions Q1's base is biased at a level about 0.6V above ground and the current through resistor R3 is set by the output voltage. If we assume that the base current is negligible, then R3's current also flows through R2, biasing Q2's collector at the positive voltage proportional to the negative output.

Q2 is connected as a diode and is used to compensate for Q1's base-emitter voltage change with temperature and collector current. Both transistors see the same collector current, and their base-emitter voltages track quite well. Because the base-emitter voltages cancel, the voltage across R2 also appears on the LT1172's feedback pin.

The resulting output voltage is given by the following formula:

$$V_{OUT} = V_{FB}\ \frac{R3}{R2}\ - V_{BE}$$

where V_{FB} is the LT1172 internal 1.244V reference, and V_{BE} is Q1's base-emitter voltage ($\approx$0.6V). The V_{BE} term in the equation denotes a minor output voltage dependency on input voltage and temperature. However, the variation due to this factor is usually well below 1%.

Essentially, Q1 holds its collector voltage constant by changing its collector current, and will function properly as long as some collector current exists. This puts the following limitation on R1: at minimum input voltage the current through R1 must exceed the current through R2. This is reflected by the following inequality:

$$R1 < R2\ \frac{V_{IN\,MIN} - V_{FB} - V_{BE}}{V_{FB}}$$

If the input voltage drops below the specified limit (e.g., under a slow start-up condition) and Q1 turns off, R4 provides the LT1172 feedback pin with a positive bias and the output voltage decreases. Without R4, the feedback pin would not get an adequate positive signal, forcing the LT1172 to provide excessive output voltage and resulting in possible circuit damage.

The feedback configuration described above is simple, yet very versatile. Only resistor value changes are required for the circuit to accommodate a variety of input and output voltages. Exactly the same feedback technique can be used with flyback, "Cuk," or inverting topologies, or whenever it is necessary to sense a negative output.

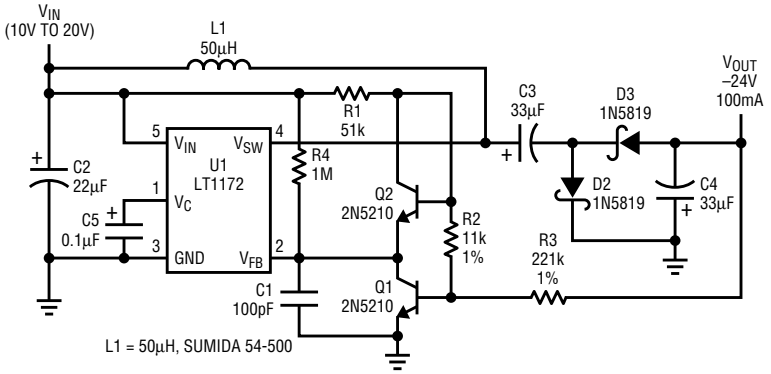


Figure 1. 10–20V to –24V converter

LT1161: ... and Back and Stop and Forward and Rest — All with No Worries at All

by Peter Schwartz
and Milt Wilcox

Many applications of DC motors require not only the ability to turn the motor on and off, but also to control its direction of rotation. When directional control is involved, the need for rapid deceleration (electronic braking) can also be assumed. A microcontroller interface (logic-level control) is a necessity in modern systems, as is protection of both the motor controller and the motor itself. With the advent of high-power, logic-level N-channel MOSFETs, it is a straightforward matter to build the lower half of an H-bridge suitable for the versatile control of DC-motor loads. Equivalent performance P-channel MOSFETs, however, are still expensive devices of limited availability, even without logic-level capability. Therefore, motor control circuits commonly use N-channel devices for the upper half of the H-bridge as well. The trick is to do this without requiring an additional power supply to provide bias for the upper MOSFET gates, while ensuring the necessary system protections.

A Complete, Six-Part Plan

The circuit shown in Figure 1 is a complete H-bridge motor driver, with six distinct modes of operation:

- ❑ Motor Forward Rotation—In this mode, Q1 and Q4 are on, and Q2 and Q3 are off.
- ❑ Motor Reverse Rotation—In this mode, Q2 and Q3 are on, and Q1 and Q4 are off.
- ❑ Motor Stop—Here, a rapid stop is performed by using "plugging braking," wherein the motor acts as a generator to dissipate mechanical energy as heat in the braking circuit's resistance.
- ❑ Motor Idle—All four MOSFETs are turned off. The motor is, in effect, disconnected from the H-bridge driver.
- ❑ Load Protect—If the motor is overloaded or stalled for an excessive period, the on-chip fault detection and protection circuitry of the LT1161 will shut the motor off for programmed interval, then turn it back on.
- ❑ Short-Circuit Protect—If a source-to-ground short is detected on either Q1 or Q2, the on-chip fault detection and protection circuitry of the LT1161 will shut off the MOSFET at risk for the programmed interval and then attempt to turn the circuit back on.

Figure 1 shows a straightforward H-bridge, using four N-channel MOSFETs (Q1–Q4). The lower MOSFETs (Q3 and Q4) are logic-level devices, to allow direct drive from 5V logic. The upper MOSFETs (Q1 and Q2) are driven via level-translation circuitry integral to the LT1161. INPUT1 of the LT1161 controls a charge pump in the IC, whose output is developed on GATE1. Similarly, INPUT2 controls a charge pump whose output is available on GATE2. The GATE outputs have voltage swings from 0V to (V_{CC} + 12V), which is more than sufficient to enhance a standard-threshold N-channel MOSFET, such as the IRFZ34. D3 is added to Q1 as a gate-source protection diode to prevent excessive voltage from appearing across the gate-source terminals of Q1. This could otherwise happen under certain conditions of "motor-idle" operation. D4 serves the same function for Q2.

The Logic Behind It All

The logic of the circuit is straightforward, and could be replaced by a microcontroller in many applications. CMOS inverters U1 and U2 drive the lower MOSFETs directly from a 5V supply, with the RCD networks on their inputs providing the necessary timing to prevent shoot-through currents in the MOSFET switches. Inverter U3 and NOR gate U5 work together to turn GATE1 and hence Q1 on when point A is at a logical high. This also ensures that C3 is charged to a logical high, to take U2's output low and turn Q3 off. Under these conditions, with point B low (or left floating), U1 will turn Q4 on and U6 will hold GATE2 and hence Q2 off. If point A is now immediately taken low (or left floating), and point B is taken high, the symmetry of the logic will reverse these conditions—but only after C3 has discharged to the point where the output of U2 can go high to turn Q3 on. This is the shoot-through prevention mentioned previously.

There are two exceptions to the symmetry of the logic: if both point A and point B are low, both upper MOSFETs are turned off while both lower MOSFETs are turned on. Under these conditions, the kinetic energy stored in the motor and its load is used to drive the motor as a generator. This produces a current through the motor winding, Q3, and Q4. In this "plugging braking" mode, the motor's energy is largely dissipated as I^2R losses, and a rapid stop occurs. If point A and point B are both high, all four MOSFETs will be turned off and the motor is essentially disconnected from the electrical circuit. Although primarily included as a cross-conduction interlock in the event that both inputs should ever be high at the same time (things do happen on the test bench), this can also be useful in situations where it is desirable that the motor coast down from a higher velocity to a lower one.

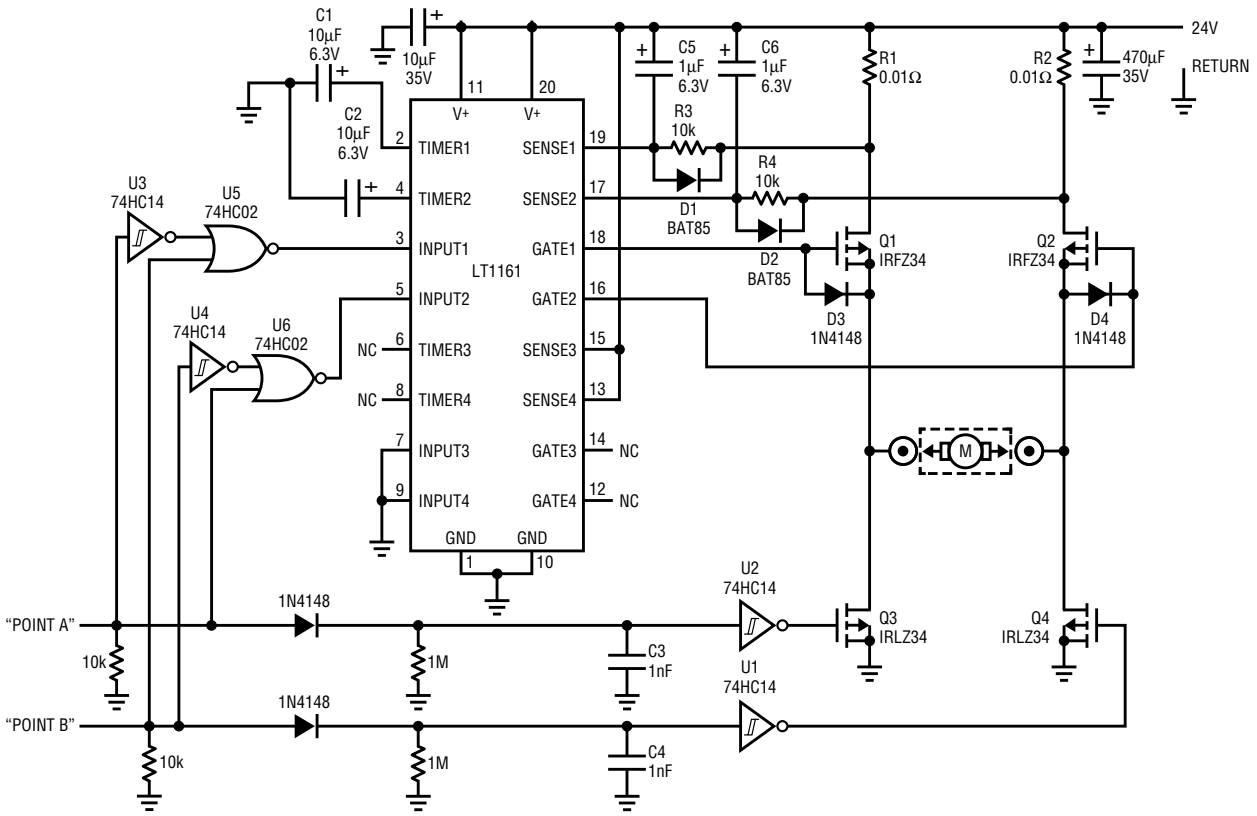


Figure 1. Schematic diagram, LT1161 based H-bridge motor driver

Just a Few Grams... but Lots of Protection

In addition to its level-translation and charge-pump features, the LT1161 also provides comprehensive protection features via its SENSE1 and SENSE2 pins. Each SENSE pin is the (–) input to an on-chip comparator, with the (+) input to that driver's comparator fixed at a level 65mV (nominal, 50mV minimum) below the LT1161's V+ input. If a SENSE pin goes more than 65mV below V+, several things happen: the corresponding GATE output is rapidly pulled to ground, the capacitor on the TIMER pin is dumped to ground, and the charge pump is shut off. The charge pump will remain shut off, and the GATE pin will remain clamped to ground, until the TIMER capacitor has charged back up to 3V from an on-chip 14µA current source. When the capacitor reaches this 3V threshold, the internal charge pump starts up again and the clamp from the GATE pin to ground is removed. The net effect of this is that, if one of the SENSE is pulled 65mV below V+, the MOSFET turns off for a period that is set by the value of the capacitor connected to the TIMER pin. At the end of this programmed interval, the circuit will automatically restart. If the fault has been cleared, the protection circuitry then becomes transparent to the system. This shutdown/retry cycle will repeat until the fault is cleared.

The fault scenarios for which protection is required are, as mentioned above, an overloaded or stalled motor, or a source-to-ground short on Q1 or Q2. In each case, such a fault will cause excessive current to flow through the affected upper MOSFET; this current is readily transformed into a voltage by a current-shunt resistor. Allowing for a 5A motor current under load, this yields a resistor value of [5A/50mV (min.)] = 0.01Ω for R1 and R2. To allow for inrush current when the motor starts up or changes direction, delay networks (R3/C5 and R4/C6) have been added to each half of the H-bridge. At a 20A startup current, the values shown give a 3ms delay. The value of the capacitor can be changed to affect longer or shorter delays as needed (the resistor value should not be raised above 10k). A short-to-ground fault, however, requires a shutdown in microseconds, not milliseconds. This is accomplished by adding two BAT85 signal-level Schottky diodes (D1 and D2) in parallel with the 10K delay resistors. At a fault current of approximately 45A, which is easily attained in the short-circuit case, V_{SHUNT} = 0.45V. At this voltage the appropriate diode conducts to temporarily bypass the delay resistor, allowing the LT1161 to turn off the imperiled MOSFET within 20µs (typical). In each case, the retry interval is programmed by C1 and C2; the 10µF shown gives a time-out of about 1.8 seconds.

The LT1161 is a quad driver IC, capable of providing drive and protection for two additional MOSFETs beyond those shown in Figure 1.

All Surface Mount EL Panel Driver Operates from 1.8V to 8V Input

by Steve Pietkiewicz

Electroluminescent (EL) panels offer a viable alternative to LED, incandescent, or CCFL backlighting systems in many portable devices. EL panels are thin, rugged, lightweight, and consume little power. They require no diffuser and emit an aesthetically pleasing blue-green light. EL panels, being capacitive in nature, typically exhibit about 3000pf per square inch of panel area and require low frequency (50Hz–1kHz) $120V_{RMS}$ AC drive. This has traditionally been generated using a low-frequency blocking oscillator with a transformer. Although this technique is efficient, transformer size renders the circuit unusable in many applications due to space constraints. Moreover, low frequency transformers are not readily available in surface-mount form, complicating assembly.

Figure 1's circuit solves these problems by using an LT1303 micropower switching regulator IC along with a small surface-mount transformer in a flyback topology. The 400Hz drive signal is supplied externally. When the drive signal is low, T1 charges the panel until the voltage at point A reaches 240VDC. C1 removes the DC component from the panel drive, resulting in +120VDC at the panel. When the input drive signal goes high, the LT1303's FB pin is also pulled high, idling the IC and turning on Q1. Q1's collector pulls point A to ground and the panel to –120VDC. C2 can be added to limit voltage if the panel is disconnected or open. R1 provides intensity control by varying output voltage. Intensity can also be modulated by varying the drive signal's frequency.

Flyback transformer T1 (Dale LPE5047-A132) has a 10 microhenry primary inductance and a 1:15 turns ratio. It measures 12mm by 13.3mm and is 6.3mm high. The 1:15 turns ratio generates high voltage at the output without exceeding the allowable voltage on the LT1303's switch pin. Schottky diode D1 is required to prevent ringing at the SW pin from forward biasing the IC's substrate diode. Because of T1's low leakage inductance, the flyback spike does not exceed 22V. No snubber network is required, since the LT1303 SW pin can safely tolerate 25V. R1 and C3 provide decoupling for the IC's VIN pin. Feedback resistor R2 is made from three 3.3MΩ units in series instead of a single 10MΩ resistor. This lessens the possibility of output voltage reduction due to PC board leakage shunting the resistor. Shutdown is accomplished by bringing the IC's SHDN pin high. For minimum current drain in shutdown, the 400Hz drive signal should be low.

Figure 3 details relevant circuit waveforms with a 22nF load (about 7 inches of panel) and a 5V input. Trace A is the panel voltage. Trace B shows switch pin action. The circuit's input current is pictured in trace C, and trace D is the 400Hz input signal. The circuit's efficiency measures about 77%. With a 5V input, the circuit can deliver 100VRMS at 400Hz into a 44nF load. More voltage can be obtained at lower drive frequencies. LT

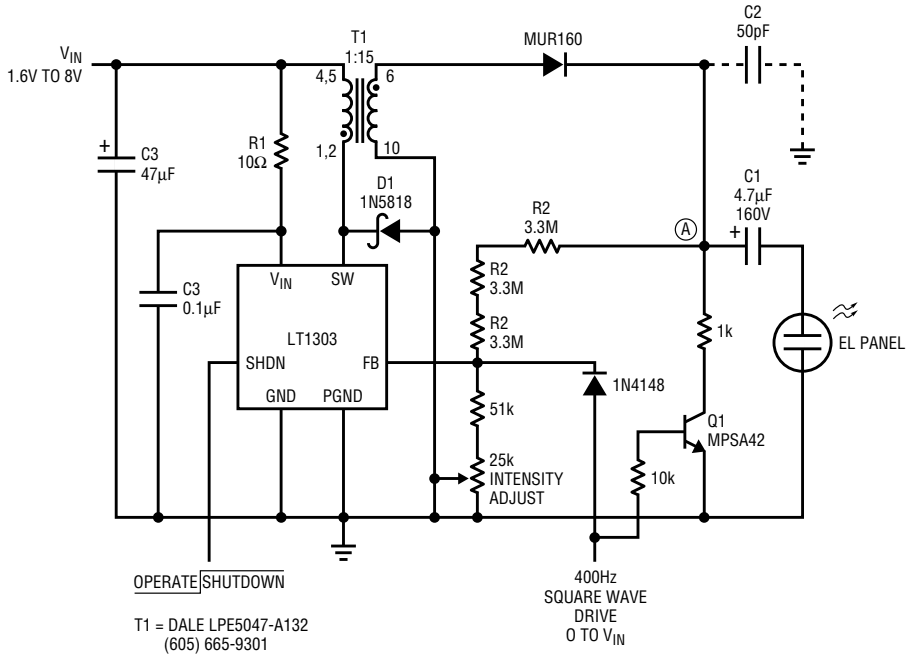
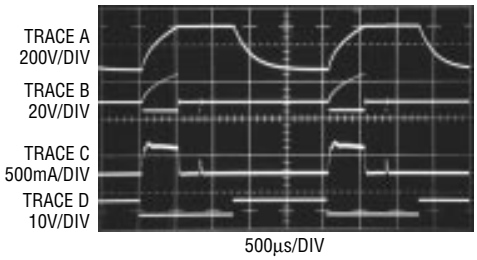


Figure 1. LT1303 circuit drives EL panel



A) HIGH VOLTAGE OUTPUT
B) SWITCH PIN
C) INPUT CURRENT
D) 400Hz DRIVE

Figure 2. Oscillograph of relevant circuit waveforms

Switching, Active GTL Terminator

by Dale Eagar

Introduction

New, high-speed microprocessors, especially those used in multiprocessor workstations and video graphics terminals, require high-speed backplanes that support peak data rates of up to 1Gbyte/second. The backplane is a passive component, whereas all drivers and receivers are implemented in low-voltage-swing CMOS (also referred to as GTL logic). These applications require bidirectional terminators, terminators that will either source or sink current (in this case, at 1.55 Volts). The current requirements of the terminator depended on the number of terminations on the backplane. Present applications may require up to 10 Amps. This specification may, of course, be reduced if required.

Circuit Operation

The complete schematic of the terminator is shown in Figure 1. The circuit is based on the LT1158 half-bridge, N-channel, power MOSFET driver. The LT1158 is configured to provide bidirectional, synchronous switching to MOSFETs Q1 through Q6. VR1, an LT1004-1.2, R1, and C1 generate a 1.25 volt reference voltage that programs the terminator's output voltage. U1A, an LT1215, is a moderate-speed (23MHz GBW), precision operational amplifier that subtracts the error voltage at its inverting input from the 1.25 volt reference. U1A is also used to amplify this error signal. Components R3 and C2 tailor the phase and gain of this section, and are selected when evaluating the system's load-step response.

U1B and part of U2 provide the gain and the phase inversion necessary to form an oscillator. C3 and C4 provide positive feedback at high frequencies, which is necessary for the system to oscillate in a controlled manner while keeping the voltage excursions within the common mode range of U1B. R8, U2, and C6 provide phase inversion and negative feed-

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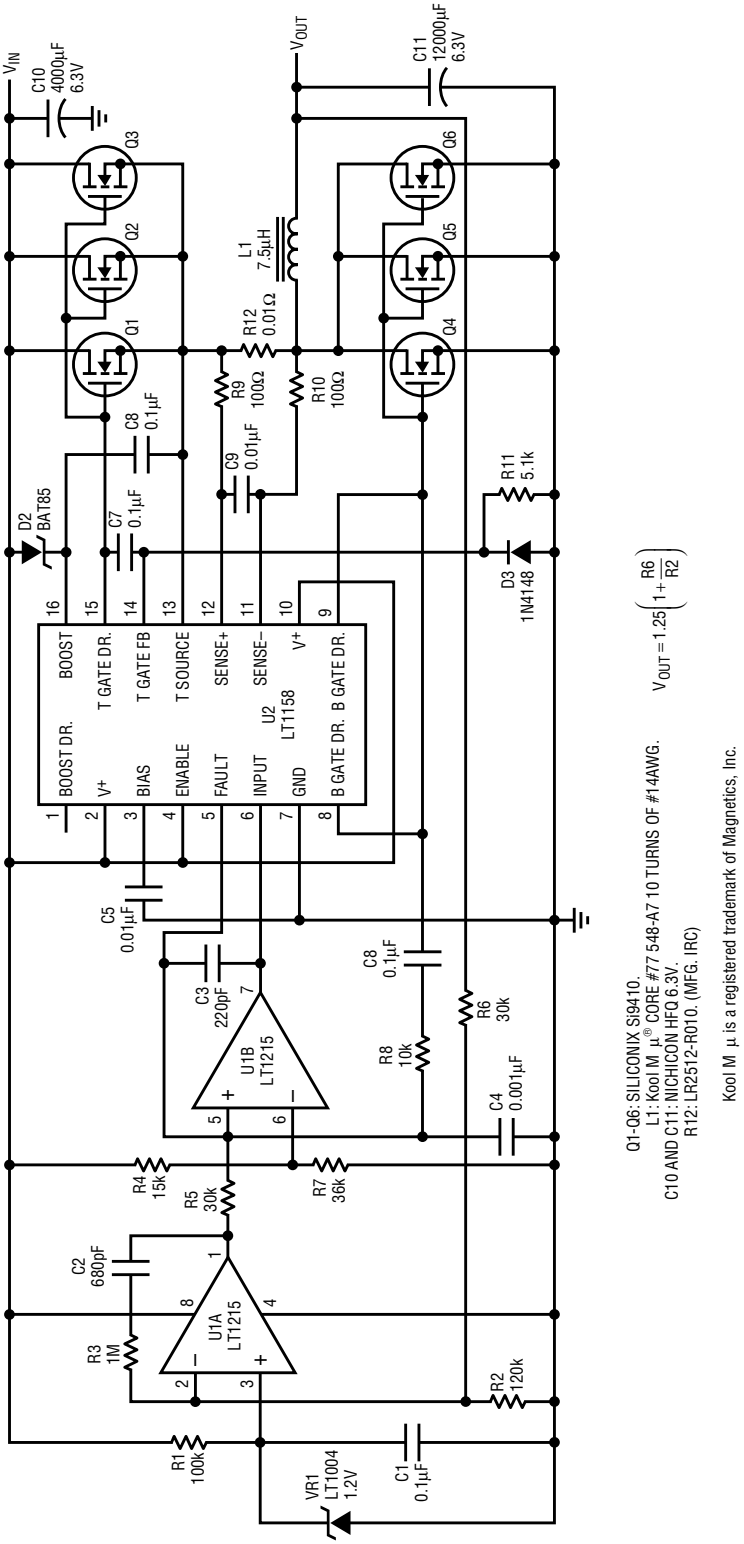

Figure 1. GTL 1.55 volt terminator provides 10 amps max. current

Automatic Load Sensing Saves Power in High-Voltage Converter

by Mitchell Lee

There are a surprising number of high-output-voltage applications for LTC's micropower DC-to-DC converter family. These applications include electroluminescent panels, specialized sensing tubes, and xenon strobes. One of the key features of the micropower converters is low quiescent current. Since the quiescent current is far less than the self-discharge rate of common alkaline cells, the traditional ON/OFF switch can be eliminated in cases where the load is intermittent, or where the load is shut down under digital control.

The maximum switch voltage for many micropower devices is 50V. For higher outputs, the circuit shown in Figure 1 is often recommended. It combines a boost regulator and a charge-pump tripler to produce an output voltage of up to 150V. The output is sensed through a divider network, which consumes a constant current of about 12µA. This doesn't seem like much, but reflected back to the 3V battery, it amounts to over 3mA. Together with the LT1107's 320µA quiescent current, the battery current is 3.5mA under no load. In standby applications this is unacceptably high, even for two D cells.

A circuit consisting of transistors Q1 and Q2 was added to reduce the standby current to an acceptable level. When a load of more than 50µA is present, Q1 turns on, Q2 turns off, and the 9.1MΩ resistor (R4) serves as a feedback path. R2, R3, and R4 regulate the output at 128V.

If the load current drops below 50µA, Q1 turns off and Q2 turns on, shorting out R4. With R4 out of the way, R2 and R3 regulate the output to approximately 15V. The measured input current under this condition is only 350µA, just slightly higher than the chip's no-load quiescent current. When the load returns, Q1 senses the excess current and the output automatically rises to its nominal value of 128V.

This automatic feedback switching scheme improves the battery current by a factor of ten and eliminates the need for a mechanical ON/OFF switch in applications where the load is under digital control. LT

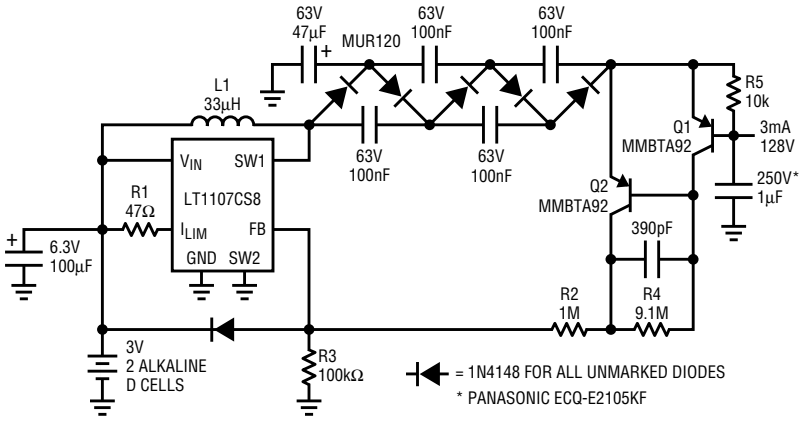

Figure 1. Automatic shutdown reduces battery current to 350 microamps

GTL, continued from page 33

back at the middle frequencies, causing U1B to oscillate at a frequency much higher than the feedback loop's response. The DC path for the oscillator is closed through the power MOSFETs Q1–Q6, the output choke L1, the output capacitor C11, and through the feedback path with the error amplifier. R4 and R7 set the center of the common-mode voltage of U1B, and are selected to limit the maximum duty factor the oscillator can achieve.

R9, R10, R12, and C9 provide output current sense to U2, allowing it to shut down the oscillator via the fault pin (pin 5) to prevent catastrophic, or even cataclysmic events from occurring. D2, C8, and the circuitry behind the boost pin (pin 16) of U2 work together to provide more than sufficient gate drive for the N-channel FETs Q1–3. D3, R11, and C7 allow the oscillator to start up regardless of the state of the oscillator on powerup.

Performance

The circuit provides excellent transient response, efficiencies in the source mode of better than 80%, and efficiencies in the sink mode of better than 90%. Figure 2 shows the step response of the terminator. LT

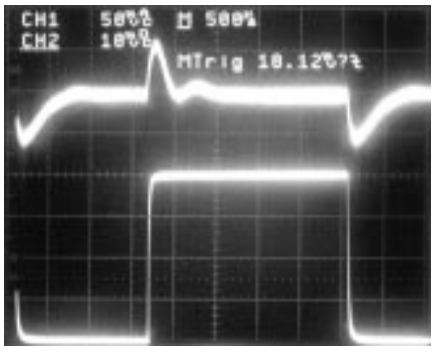

Figure 2. Step response of LT1158-based terminator

High-Efficiency 12V to –12V Converter

by Milton Wilcox and Christophe Franklin

It is difficult to obtain high efficiencies from inverting switching regulators because the peak switch and inductor currents must be roughly twice the output current. Furthermore, the switch node must swing twice the input voltage (24V for a 12V inverting converter). The adjustable version of the LTC1159 synchronous stepdown controller is ideally suited for this application, producing a combination of better than 80% efficiency, low quiescent current, and 20µA shutdown current.

The 1A circuit shown in Figure 1 exploits the high input-voltage capability of the LTC1159 by connecting the controller ground pins to the –12V output. This allows the simple feedback divider between ground and the output (comprising R1 and R2) to set the regulated voltage, since the internal 1.25V reference rides on the negative output. The inductor connects to ground via the 50mΩ current-sense resistor.

A unique EXT V_{CC} pin on the LTC1159 allows the MOSFET drivers and control circuitry to be powered from the output of the regulator. In Figure 1 this is accomplished by grounding EXT V_{CC}, placing the entire 12V output voltage across the driver and control circuits (remember, the ground pins are at –12V). This is permissible with the LTC1159, which allows a maximum of 13V between the sense and ground pins. During start-up or short-circuit conditions, operating power is supplied by an internal, 4.5V low-dropout linear regulator. This start-up regulator automatically turns off when the output falls below –4.5V.

A cycle of operation begins when Q1 turns on, placing the 12V input across the inductor. This causes the inductor current to ramp to a level set by the error amplifier in the LTC1159. Q1 then turns off and Q2 turns on, causing the current stored in the inductor to flow to the –12V output. At the end of the 5µs off-time (set by capacitor C_T), Q2 turns off and Q1 resumes conduction. With a +12V input, the duty cycle is 50%, resulting in a 100kHz operating frequency.

The LTC1159, like other members of the LTC1148 family, automatically switches to Burst Mode operation at low output currents. Figure 1's circuit enters Burst Mode operation below approximately 200mA of load current. This maintains operating efficiencies exceeding 65% over two decades of load current range, as shown in Figure 2. Quiescent current (measured with no load) is 1.8mA.

Complete shutdown is achieved by pulling the gate of Q3 low. Q3, which can be interfaced to either 3.3V or 5V logic, creates a 5V shutdown signal, referenced to the negative output voltage, to activate the LTC1159 shutdown2 pin. Additionally, Q4 offsets the VFB pin to ensure that Q1 and Q2 remain off during the entire shutdown sequence. In shutdown conditions, 40µA flows in Q3 and only 20µA is taken from the +12V input.

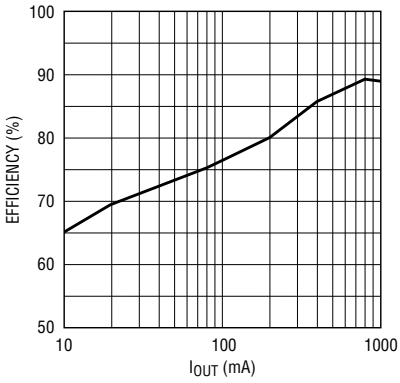

Figure 2. Efficiency plot of Figure 1's circuit

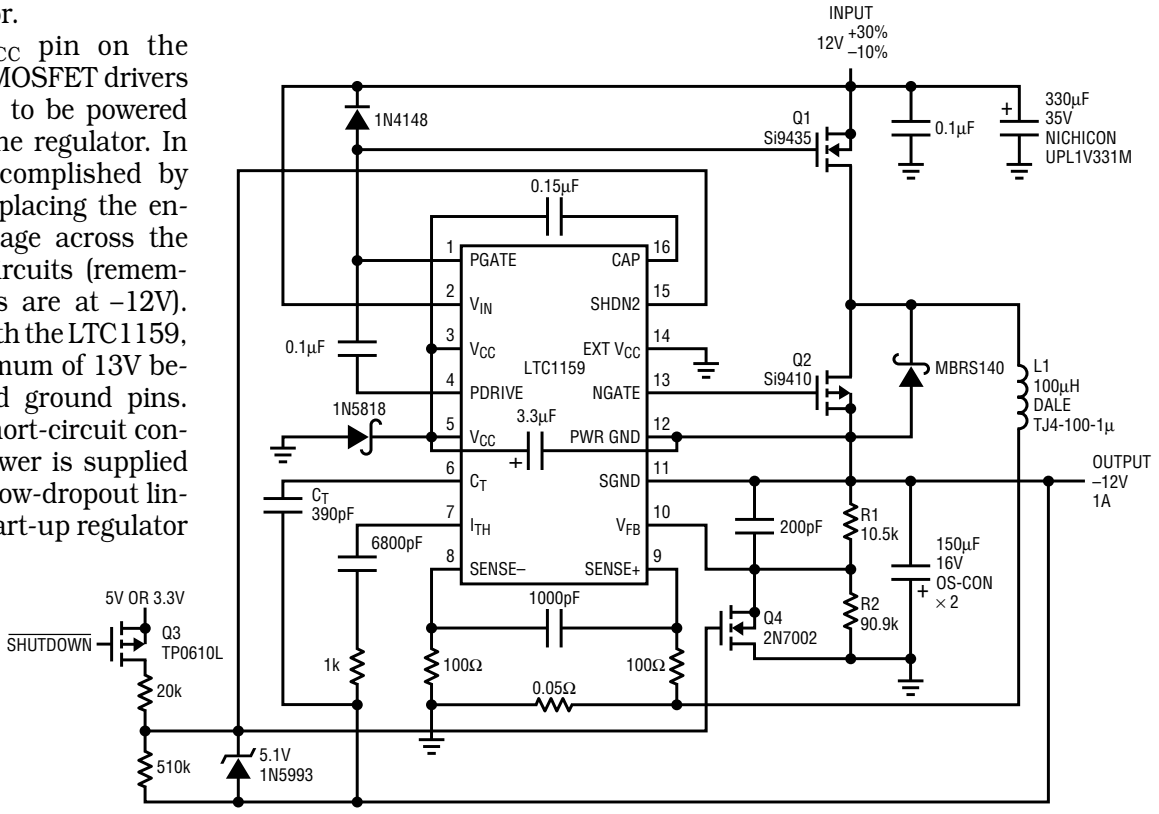

Figure 1. LTC1159 converts 12V to –12V at 1 Amp

LT1251 Circuit Smoothly Fades Video to Black

by Frank Cox

When a video signal is attenuated there is a point were the sync amplitude is too small for a monitor to process properly. Instead of making a smooth transition to black, the picture rolls and tears. One solution to this problem is to run a separate sync signal into the monitor. This may not be a viable solution in a system where cost and complexity are the prime concerns. What is needed is a simple video "volume control."

The circuit in Figure 1 can perform a smooth fade to black, while maintaining good video fidelity. U1, an LT1360 op amp, and its associated components, form an elementary sync separator. C1, R1 and D1 clamp the composite video. D2 biases the input of U1 to compensate for the drop across D1. When D1 conducts, the most negative portion of the waveform, containing the sync information, is amplified by U1. The clamp circuit in the feedback network of U1 (D4–D8) prevents the amplifier from saturating. D3 and the CMOS inverter U4 complete the shaping of the sync waveform. This sync separator works with most video signals but, because of its simplicity, will not work with very noisy or distorted video. The remainder of the circuit is an LT1251 video fader (U2) configured to fade between the original video and the sync stripped from that video. Thus, the video fades to black.

The control voltage for the fader is generated by a voltage reference and a 10kΩ variable resistor. If this control potentiometer is mounted an appreciable distance from the circuit or if the control generates any noise when adjusted, this node should be bypassed.

Figure 2 is a multiple-exposure waveform photograph that shows the action of this circuit. Two linear-ramp video test signals are shown in this photograph. The video is faded from full amplitude to zero amplitude in six steps. The sync waveform (lower center) remains unchanged. In Figure 3, a single video line modulated with color subcarrier is faded from full video amplitude to zero video amplitude. The monitor will eventually lose color lock and shut the color off as the amplitude of the color subcarrier is reduced. This is not a problem in this application because the color decoding circuits in the monitor are designed to work with a variety of signals from tape or broadcast, and so have a large dynamic range. Color portions of the picture will remain after the luminance portion is completely black. LT

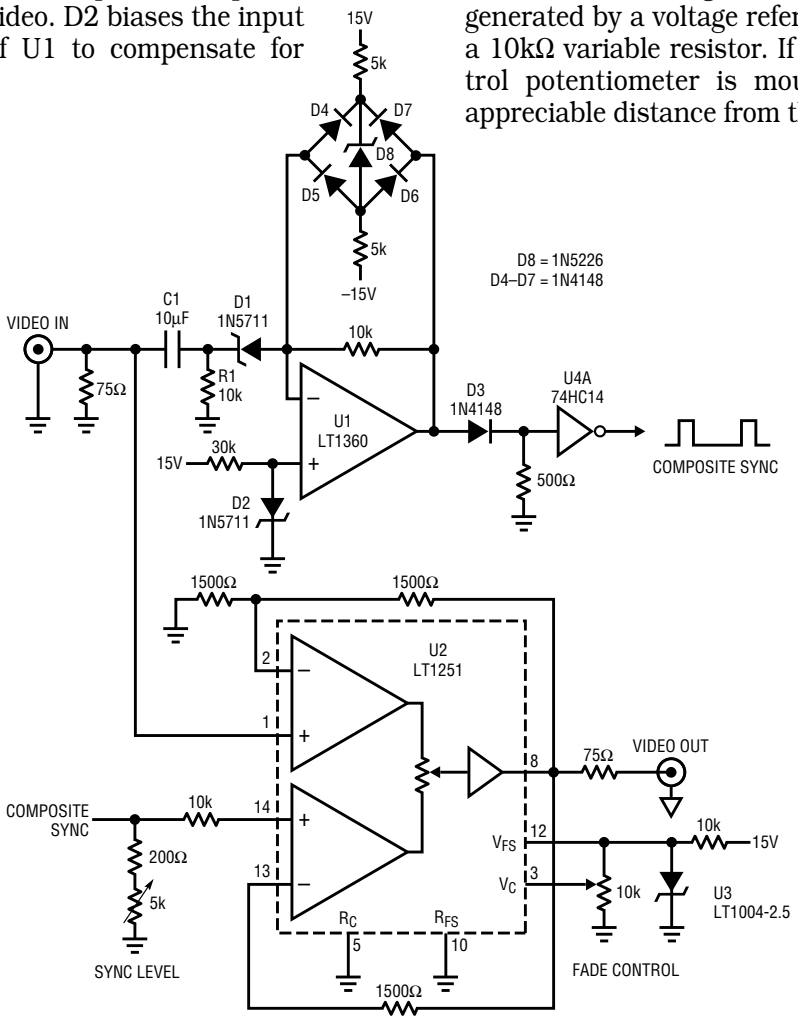

Figure 1. Schematic diagram LT1251 video fader

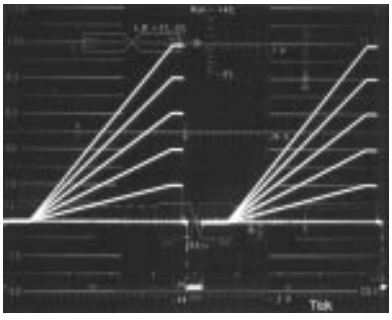

Figure 2. Multiple-exposure photo showing circuit operation

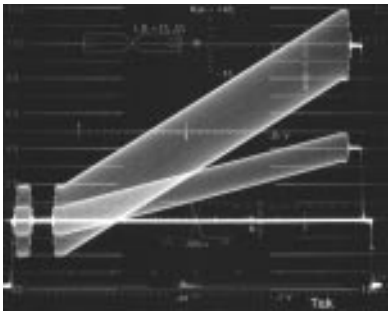

Figure 3. Photo detailing a single video line with color subcarrier faded to zero amplitude

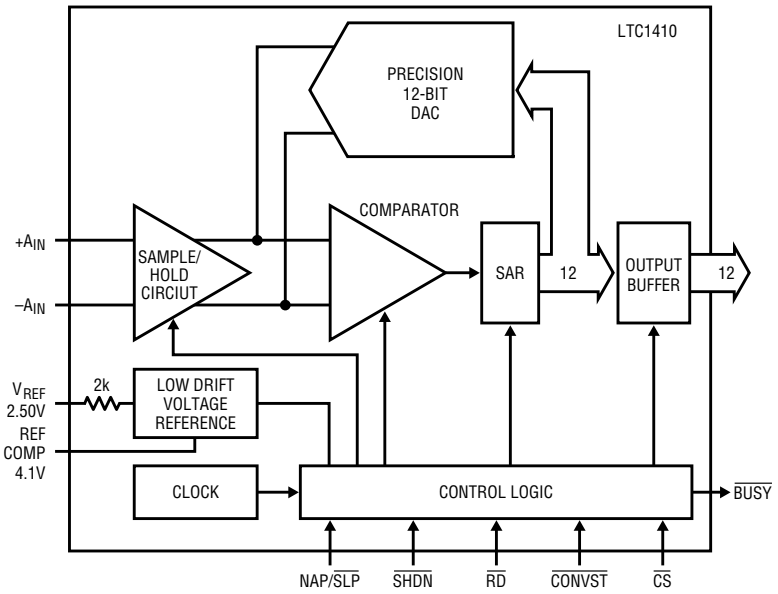

Figure 1. LTC1410 block diagram

LTC1410 , continued from page 1

adding any DC errors due to on-resistance. The low input capacitance (10pF) allows fast acquisition time for the sample-and-hold, even with high source impedance.

Good DC performance of the ADC is critical, since it limits the performance of the entire system. The LTC1410 is guaranteed to have 0.8LSB maximum differential linearity error and no more than 0.5LSB of integral linearity error. The low gain and offset errors remain nearly constant with power-supply and temperature variations, so that they can be easily corrected in software or nulled out with simple external circuitry. Low code-transition noise results in stable readings and reduces the need for averaging, further improving system speed. (Code-transition noise is the uncertainty in the location of a code transition edge. A noisy part might have 0.5LSB $_{RMS}$ noise, whereas a quiet part might have 0.05 to 0.1LSB $_{RMS}$.)

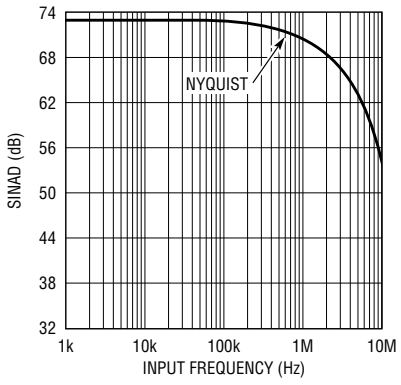

Figure 2. Signal-to-noise plus distortion (SINAD) versus sampling frequency

The internal reference of the LTC1410 is set at 2.5V, so that it is compatible with many system references. With a temperature coefficient of 10ppm/°C, it can serve as the master reference for the system, so that all other analog circuits in the system track the same reference. If an external reference circuit is to be used as the master, the resistive (2kΩ) reference output can easily be overdriven with an external 2.5V reference.

Perfect for Telecommunications

Telecommunications applications such as HDSL, direct down conversion, and modems, require high dynamic performance, since the ADC must sample high-frequency AC signals. The sample-and-hold must accurately track the input signal without adding any distortion or noise. A key measure of dynamic performance for a sampling ADC is the signal-to-noise plus distortion ratio, often abbreviated as SINAD. In an ideal ADC there would be no distortion or noise and the SINAD would be limited only by the resolution of the ADC; for 12 bits, the ideal SINAD is 74.01dB. Figure 2 shows the SINAD for the LTC1410 as a function of input frequency. Note that the SINAD is 72dB for input frequencies below 100kHz, only 2dB lower than ideal. At the Nyquist frequency the SINAD is only 2dB lower than at DC.

Another important requirement for telecommunications systems is a low error rate. In any ADC there is a finite probability that a large conversion error (greater than 1% of full scale) will occur. In video or flash converters, these large errors are called "sparkle codes." Large errors are problems in telecommunications systems such as HDSL, since they result in data transmission errors. All ADCs have a rate at which errors occur, referred to as the error rate. The error rate depends on the ADC architecture, design, and process. Error rates vary greatly and can be lower than one in ten billion or as high as one in one million. Telecommunications systems typically require error rates of one in one billion or better.

The LTC1410 is designed to have ultra-low error rates. The error rate is so low that it is difficult to measure because of the time between errors. To make measurement more practical, the error rate was measured at an elevated temperature of 150°C (error rate increases with temperature). Even at this high temperature the error rate was one in 100 billion. The projected error rate at room temperature is one in 2,000,000 billion, or about one error every 50 years running at full conversion rate.

Differential Inputs Ignore Common-Mode Noise

Getting a clean signal to the input(s) of an ADC is not an easy task in many systems. Large noise signals from EMI, the AC power line, and digital circuitry are usually present. Filtering and shielding are the common techniques for reducing noise, but these are not always adequate. The LTC1410 offers another tool to fight noise, differential inputs.

Figure 3a depicts a typical single-ended sampling system with ground noise, which may be 60Hz noise, digital clock noise, or some other type of

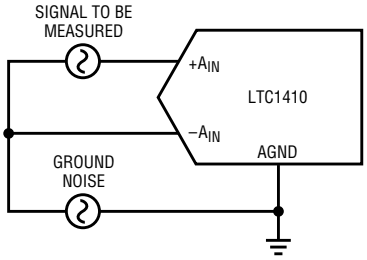

Figure 3a. Single-input ADC measuring a signal riding on common-mode noise

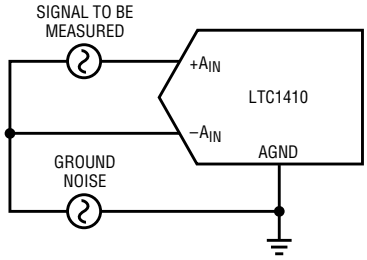

Figure 3b. Differential-input ADC measuring a signal riding on common-mode noise

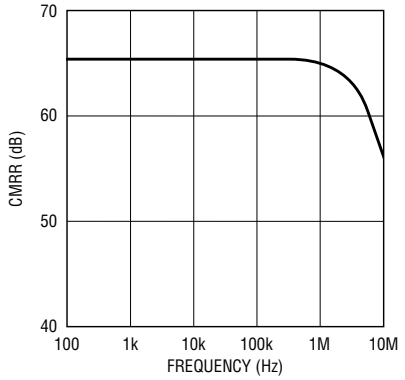

Figure 4. LTC1410 CMRR versus frequency

noise. When a single-ended input is used, the ground noise adds directly to the input signal. By using the differential inputs of the LTC1410 the ground noise can be rejected by connecting the inputs directly across the signal of interest, as shown in Figure 3b. Ground noise becomes "common mode" and is rejected internally by the LTC1410 by virtue of its excellent common-mode rejection ratio (CMRR). Figure 4 shows the CMRR of the LTC1410 versus frequency. Notice that the CMRR is constant over the entire Nyquist bandwidth, and is only 3dB lower at 5MHz. This ability to reject high-frequency common-mode signals is very helpful in sampling systems where noise often has high-frequency components due to switching transients.

Low-Power Applications

LTC1410 is especially well suited for applications that require low power and high speed. The normal operating power is low—only 150mW. Power may be further reduced if there are extended periods of time between conversions. During these inactive periods, when the ADC is not converting, the LTC1410 may be shut down. There are two power shutdown modes: NAP and SLEEP modes.

NAP mode shuts down 95% of the power and leaves only the reference and logic powered up. Wake-up from NAP mode is extremely rapid; in 100ns the LTC1410 can go from NAP mode to converting. In NAP mode, all data output control is functional; data from the last conversion prior to starting NAP mode can be read during NAP mode. $\overline{RD}$ and $\overline{CS}$ also control the state of the output buffers. NAP mode is useful for applications that must immediately take data after long inactive periods.

SLEEP mode is used when the NAP-mode current drain is too high or if wake-up time is not critical. In SLEEP mode, all bias currents are shut down, the reference is shut down, and the logic outputs are put in a high-impedance state. The only current that remains is junction-leakage current, less than 1µA. Wake-up from the SLEEP mode is much slower, since the reference circuit must power up and settle to 0.01% for full accuracy. The wake-up time also depends on the value of the compensation capacitor used on the REF COMP pin. With the recommended 10µF capacitor the wake-up time is 10ms. SLEEP mode is useful for inactive periods greater than 10ms.

Conclusions

The new LTC1410 high-speed, 12-bit ADC will find uses in many types of dynamic sampling applications. These include high-speed telephony, compressed video, and dynamic data acquisition. The LTC1410 improves on both the AC and DC performance of hybrids, and its monolithic construction improves power dissipation, cost, and reliability. LT

LT1175, continued from page 14

even with extremely low output-capacitor ESR.

The end result of all this attention to loop stability is that the output capacitor used with the LT1175 can range in value from 0.1µF to hundreds of microfarads, with an ESR of 0–5Ω. This allows the use of ceramic, solid tantalum, aluminum, or film capacitors over a wide range of values.

High-Temperature Operation

The LT1175 is a micropower design, with only 45 microamperes of quiescent current. This could make it perform poorly at high temperatures (>125°C), where power-transistor leakage might exceed the output-node loading current (5–15µA). To avoid a condition where the output voltage drifts high during a high-temperature, no-load condition, the LT1175 has an active load, which turns on when the output is pulled above the correct regulated voltage. This absorbs power-transistor leakage and maintains good regulation. There is one downside to this feature, however. If the output is pulled high deliberately, as it might be when the LT1175 is used as a backup to a slightly higher output from a primary regulator, the LT1175 will act as an unwanted load on the primary regulator. Because of this, the active pull-down is deliberately "weak." It can be modeled as a 2kΩ resistor in series with an internal-clamp voltage when the regulator output is being pulled high. For example, if a 4.8V output is pulled to 5V, the load on the primary regulator would be (5V –4.8V)/2kΩ = 100µA. This also means that if the internal pass transistor leaks 50µA, the output voltage will be (50µA)(2kΩ) = 100mV high. This condition will not occur under normal operating conditions, but could occur immediately after an output short circuit that overheated the chip. LT

New Device Cameos

LTC1177 Isolated, High-Side Driver

The LTC1177 isolated high-side driver is targeted at telecommunications, power supply, line-operated, intrinsically safe, and RF-control applications. It provides isolated gate drive for floating MOSFETs at voltages up to 2.5kV. Among many possible uses, it can drive a pair of back-to-back MOSFET switches as a fully isolated AC line relay. The LTC1177 outperforms photoMOS relays in most applications, since it can drive large, low-resistance FETs with far less input current.

To simplify designs, a current limiter and active turn-off circuit are included on chip. Input current to operate the chip is 2.5mA, and stray coupling from input to output is only 2pF, limiting leakage currents from 117V circuits to less than 100nA. The LTC1177 is supplied in both DIP and SO packages; samples are available now.

The LT1319: A Low-Noise, High-Speed Photodiode Amplifier for Infrared Data Transmission

The LT1319 is a general-purpose infrared receiver that converts current from a photodiode to a digital signal. It is designed to easily provide IR communications between portable computers, personal digital assistants (PDAs), desktop computers, and peripherals such as printers. The LT1319 supports low-speed standards such as Infrared Data Association (IrDA) and Sharp/Newton, as well as the emerging faster data rate standards above 1MBaud.

Key features of the LT1319 include a low-noise, high-speed preamplifier for high data rates at long distances, AC coupling loops that reject ambient interference, two gain channels and two comparators to detect multiple standards, single 5V supply operation, a power-saving shutdown feature, and a 16-lead SOIC package.

The LT1319 consists of a photodiode preamplifier followed by two separate gain channels and comparators. The preamplifier converts the current from an external photodiode to a voltage and has a transimpedance gain internally set to 13kΩ. The bandwidth of the preamp is 6MHz, which allows reception of very high data rates. The input-referred noise is a low 2pA Hz, which provides high sensitivity and therefore greater transmission distances. A highpass filter loop within the preamp rejects ambient interference. The cutoff frequency of this loop is easily adjustable with a capacitor to ground. After further external filtering, which can be tailored to the desired communication standards, two channels with high input impedance and a gain of 400V/V amplify the signal and drive comparators with adjustable thresholds. One comparator has a response time of 25ns and is well suited for data rates up to 4MBaud or high-frequency, carrier-based modulation methods. The second comparator has a 60ns response time and is useful for more modest data rates such as in the IrDA and Sharp/Newton standards. The gain stages also contain highpass filter loops for further ambient rejection. A shutdown feature reduces power from 14mA to 500µA.

LTC1574 High-Efficiency Step-Down DC/DC Converter with Internal Schottky Diode

The new LTC1574 requires only three external components, an inductor and two capacitors, to construct a space saving, efficient step-down DC/DC converter with better than 90% efficiency. With its internal low $R_{DS(ON)}$ switch (0.9Ω at a supply voltage of 12V) and low forward drop Schottky diode (0.390V at 200mA), external components are minimized, leaving only the input capacitor, output capacitor, and a small surface-mount inductor. The LTC1574 features a wide 4V-to-18.5V input operating-voltage range with minimal supply currents. Under a no-load condition, the LTC1574 draws only 130µA. In shutdown mode, it draws a mere 2µA, making this converter ideal for battery powered applications. In dropout mode, the internal P-channel MOSFET switch turns on continuously, providing extremely low dropout specifications (better than those of most linear regulators). This allows the user to maximize the life of the battery.

The LTC1574 step-down converter is designed specifically to eliminate noise at audio frequencies, while maintaining high efficiency at low output currents. The internal switch is current controlled at a peak of approximately 340mA or 600mA, selectable by a control pin. Low peak switch current is one of the key features that allow the LTC1574 to minimize system noise compared to other devices that carry significantly higher peak currents. This eases shielding and filtering requirements and decreases component stresses. Output currents of up to 450mA are possible with this device when the $I_{PROGRAM}$ pin is connected to V_{INPUT}, increasing the peak current to 600mA.

The LTC1574 is available in fixed 5V, fixed 3.3V, and adjustable versions in the 16-lead narrow SOIC package. LT

For further information on the above or any of the other devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number: 1-800-4-LINEAR. Ask for the pertinent data sheets and application notes.

DESIGN TOOLS

Applications on Disk

NOISE DISK
This IBM-PC (or compatible) progam allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate noise using specs for any op amp. Available at no charge.

SPICE MACROMODEL DISK
This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models, and a demonstration copy of PSPICE™ by MicroSim. Available at no charge.

Technical Books

1990 Linear Databook — This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook Supplement — This 1248 page supplement to the *1990 Linear Databook* is a collection of all products introduced since then. The catalog contains full data sheets for over 140 devices. The *1992 Linear Databook Supplement* is a companion to the *1990 Linear Databook*, which should not be discarded. $10.00

1994 Linear Databook, Volume III — This 1826 page supplement to the *1990 Linear Databook* and *1992 Linear Databook Supplement* is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The *1994 Linear Databook Volume III* is a supplement to the 1990 and 1992 Databooks, which should not be discarded. $10.00

Linear Applications Handbook — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22 page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook Volume II — Continues the stream of "real world" linear circuitry initiated by the *1990 Handbook*. Similar in scope to the 1990 edition, the new book covers Application Notes 41 through 54 and Design Notes 33 through 69. Additionally, references and articles from non-LTC publications that we have found useful are also included. $20.00

Interface Product Handbook — This 336 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, 10kV ESD protection of RS232 devices and surface mount packages. Available at no charge.

Monolithic Filter Handbook — This 234 page book comes with a disk which runs on PCs. Together, the book and disk assist in the selection, design and implementation of the right switched capacitor filter circuit. The disk contains standard filter responses as well as a custom mode. The handbook contains over 20 data sheets, Design Notes and Application Notes. $40.00

SwitcherCAD Handbook — This 144 page manual, including disk, guides the user through SwitcherCAD—a powerful PC software tool which aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. $20.00

1994 Power Solutions Brochure — This 52 page collection of circuits contains real-life solutions for common power supply design problems. There are over 45 circuits, including descriptions, graphs and performance specifications. Topics covered include micropower DC/DC, step-up and step-down switching regulators, off-line switching regulators, linear regulators, switched capacitor conversion and power management. Available at no charge.

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